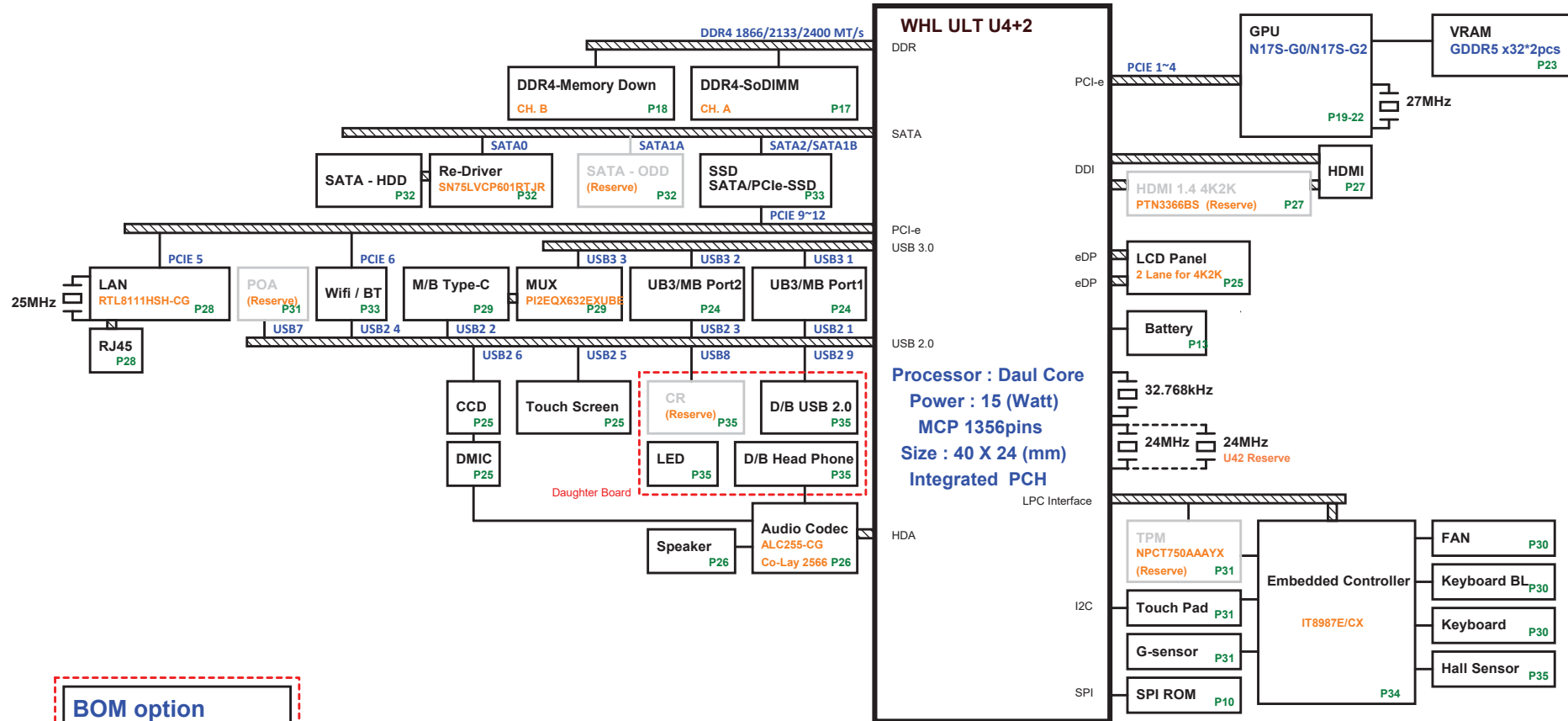


ZAW Whiskey Lake series Platform Block Diagram (DIS/UMA)

01

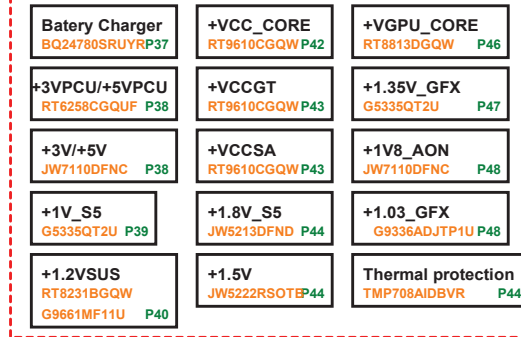


BOM option

IV@ : UMA
EV@ : DIS
TPC@ : Type-C function
TPC_N@ : No Type-C function
TSI@ : Touch screen I2C
TPM@ : Trusted Platform Module
PBA@ : Finger Print on touch pad
KBL@ : Keyboard back light
GS@ : G-Sensor function
GS_N@ : No G-Sensor function
SSD@ : Solid State Disk
ODD@ : Optical Disc Drive
EMC@ : eMMC function
RAM@ : On Board Memory
SP@ : Power & VGA
HDD_R@ : Hard Disc Redriver
HDD_N@ : NO Hard Disc Redriver
CNV@ : Intel WIFI
CNV_N@ : NO Intel WIFI
HDMI_R@ : HDMI Redriver
HDMI_N@ : No HDMI Redriver
Debug@ : for Debug Card
255@ : Codec 255
256@ : Codec 256

FOR15~17@ : Panel 15 or 17 inch
FOR14@ : Panel 14 inch

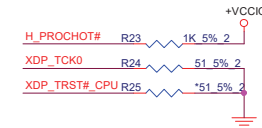
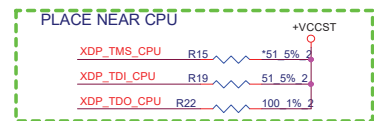
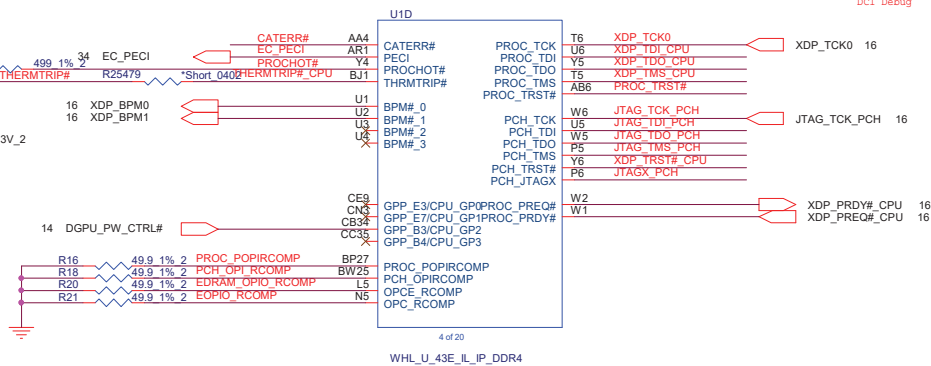
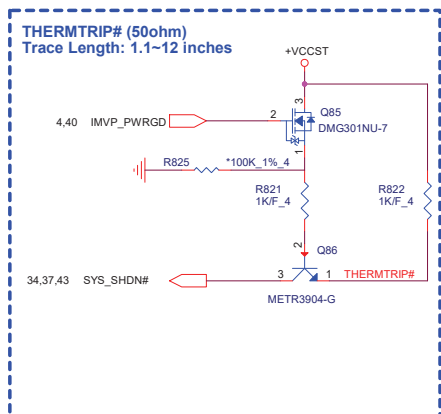
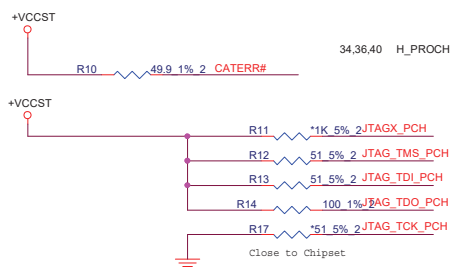
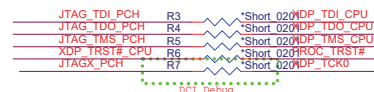
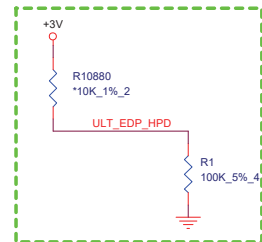
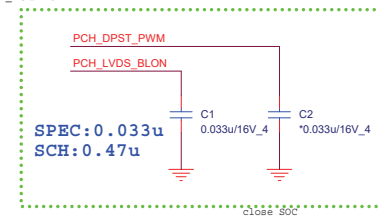
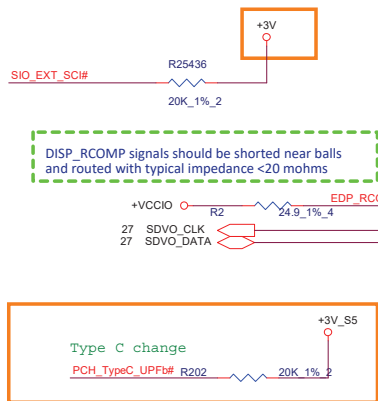
Power solution



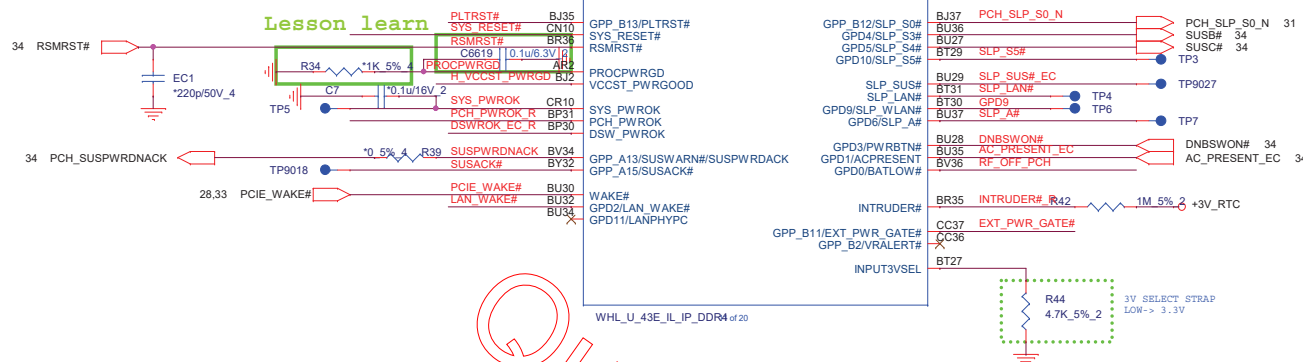
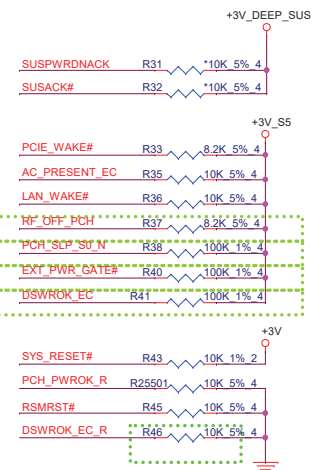
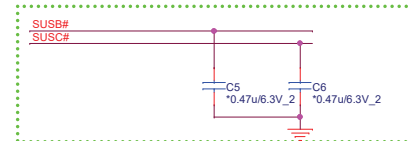
PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT

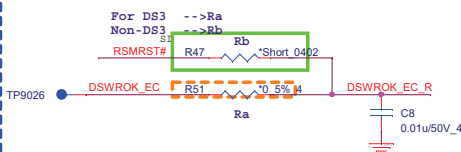
HDMI



PCH Pull-high/low(CLG)

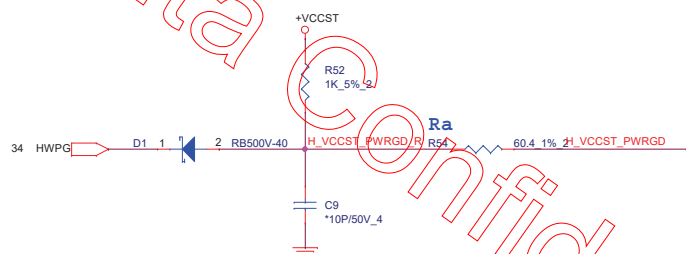
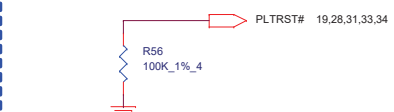


For DS3 Sequence

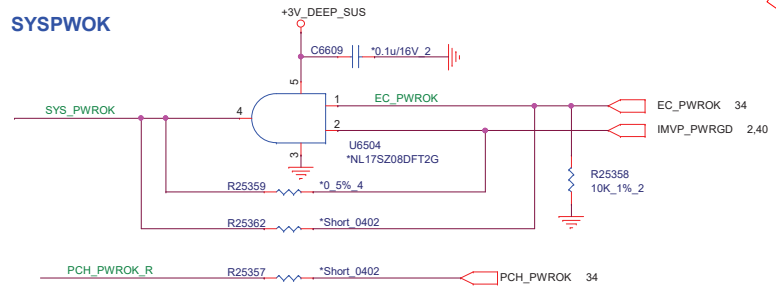


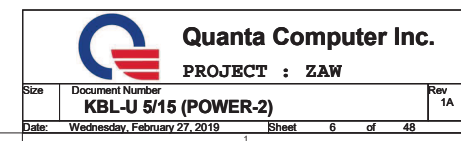
PLTRST#(CLG)

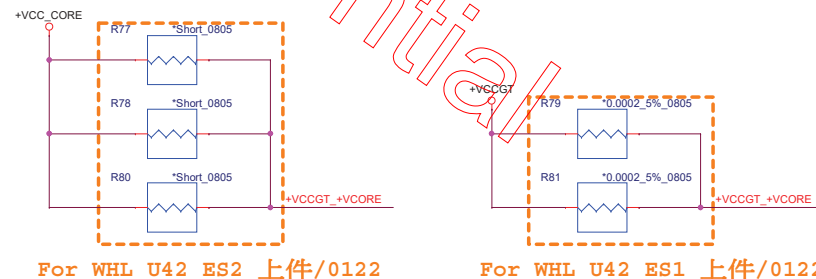
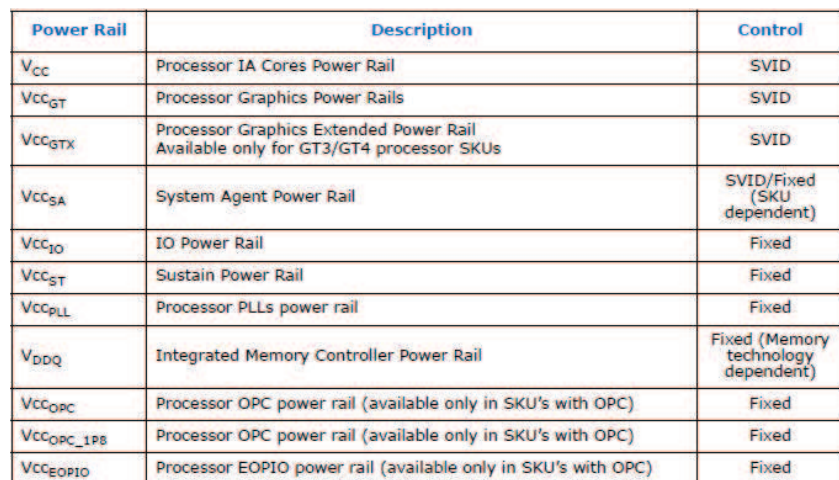
Check Rise/Fall time less than 100ns

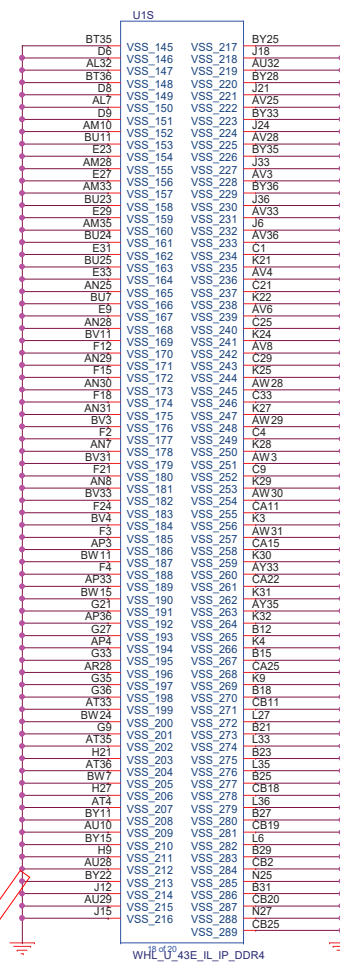
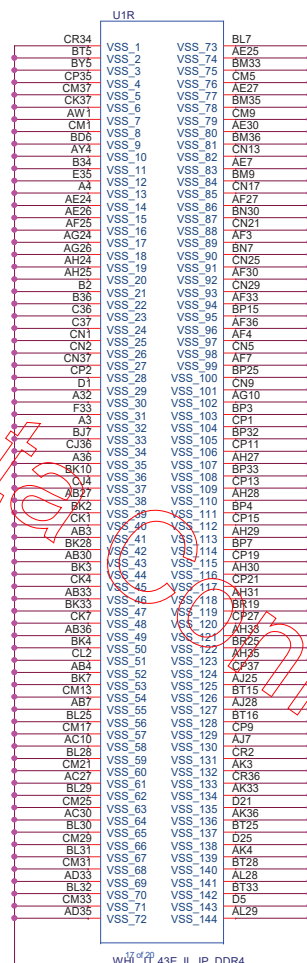
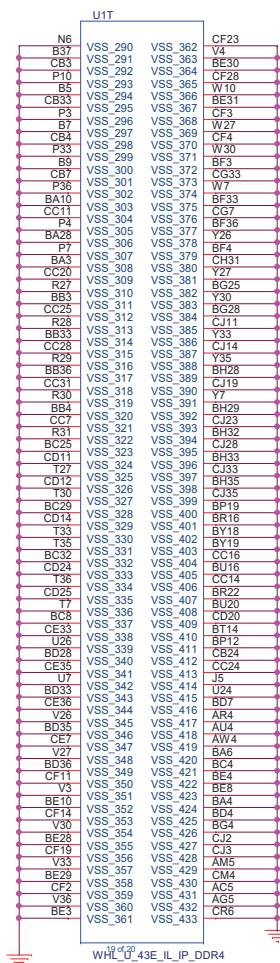
Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

SYSPWOK





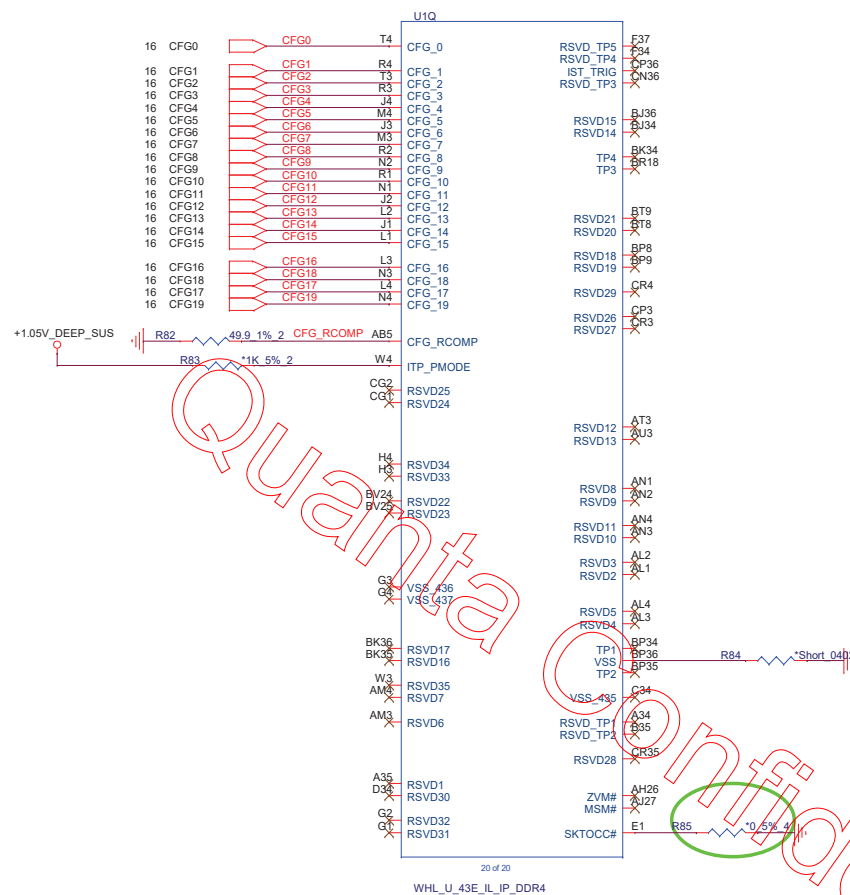




Quanta Computer Inc.

PROJECT : ZAW

Size	Document Number	Rev
	KBL-U 7/15 (GND)	1A
Date:	Wednesday, February 27, 2019	Sheet 8 of 48



Vinafix

Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

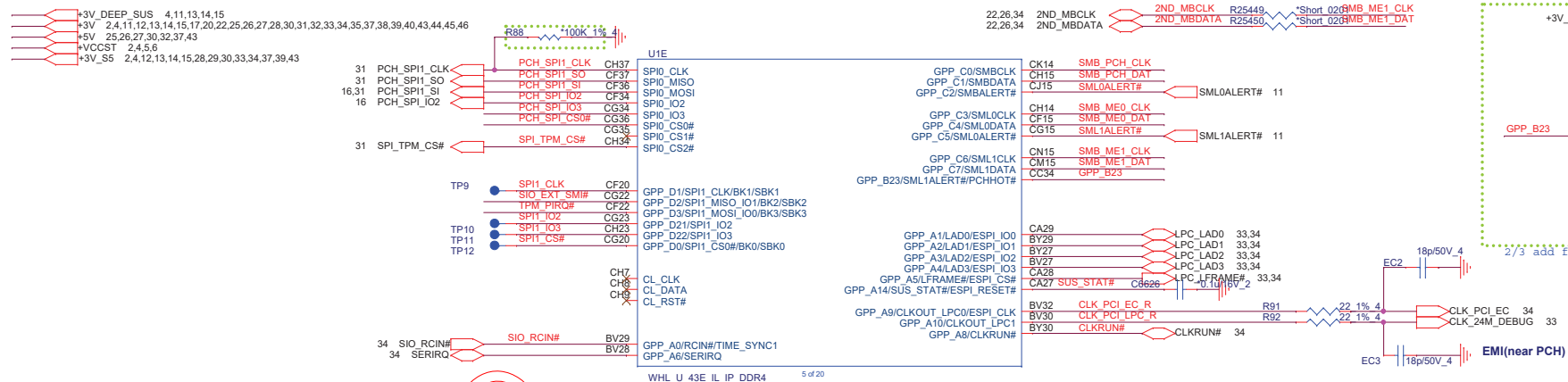


Quanta Computer Inc.

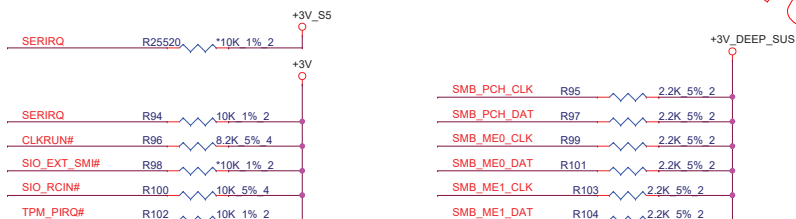
PROJECT : ZAW

Size	Document Number	Rev
	KBL-U 8/15 (RSV)	1A

Date: Wednesday, February 27, 2019 Sheet 9 of 48



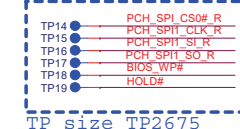
GPIO Pull UP



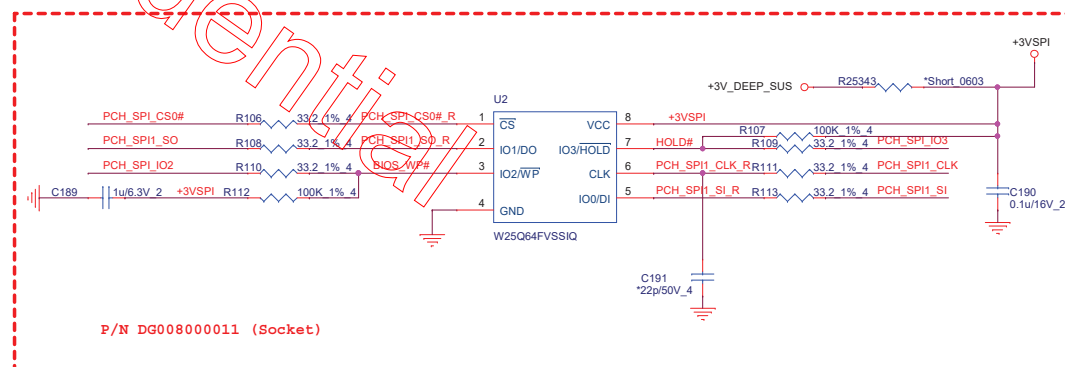
PCH SPI ROM(CLG)

Vender		Size	P/N	
Kabylake POA 3.3V	MXIC	16M	AKE3DZN0Z03	MX25L12873FM2L-10
	Winbond	16M	AKE3DF-KN01	W25Q128JVSQ
	GigaDevice	16M	AKE3DZN0Q02	GD25B127DSIGR

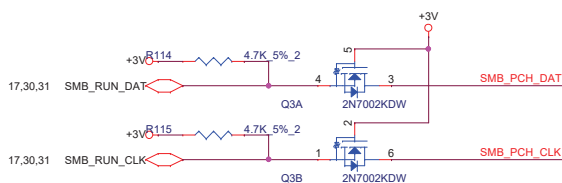
need place to TOP



PCH SPI ROM(CLG)



SMBus/Pull-up(CLG)

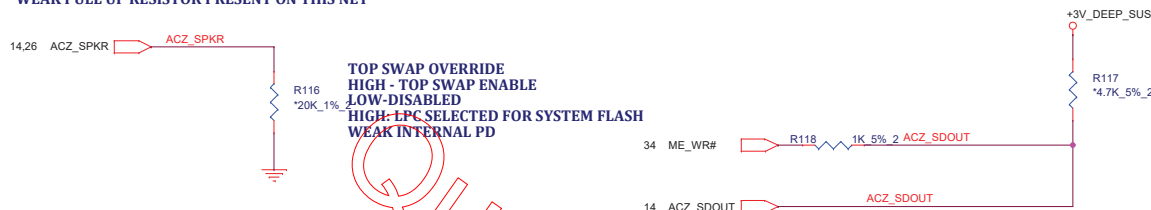


CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR4

Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



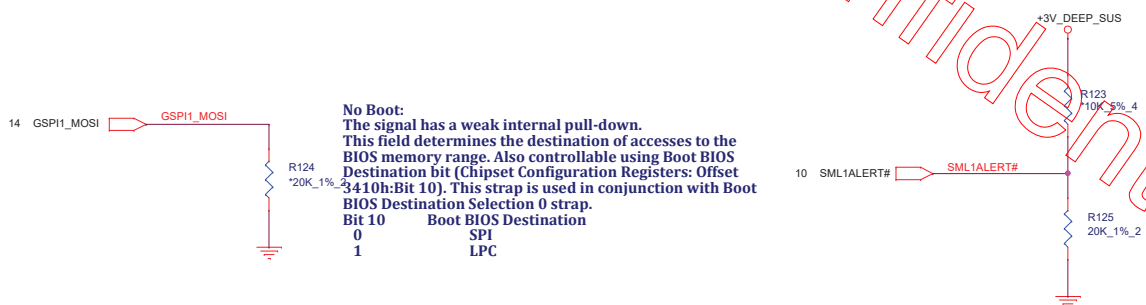
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW - DISABLED
HIGH - LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



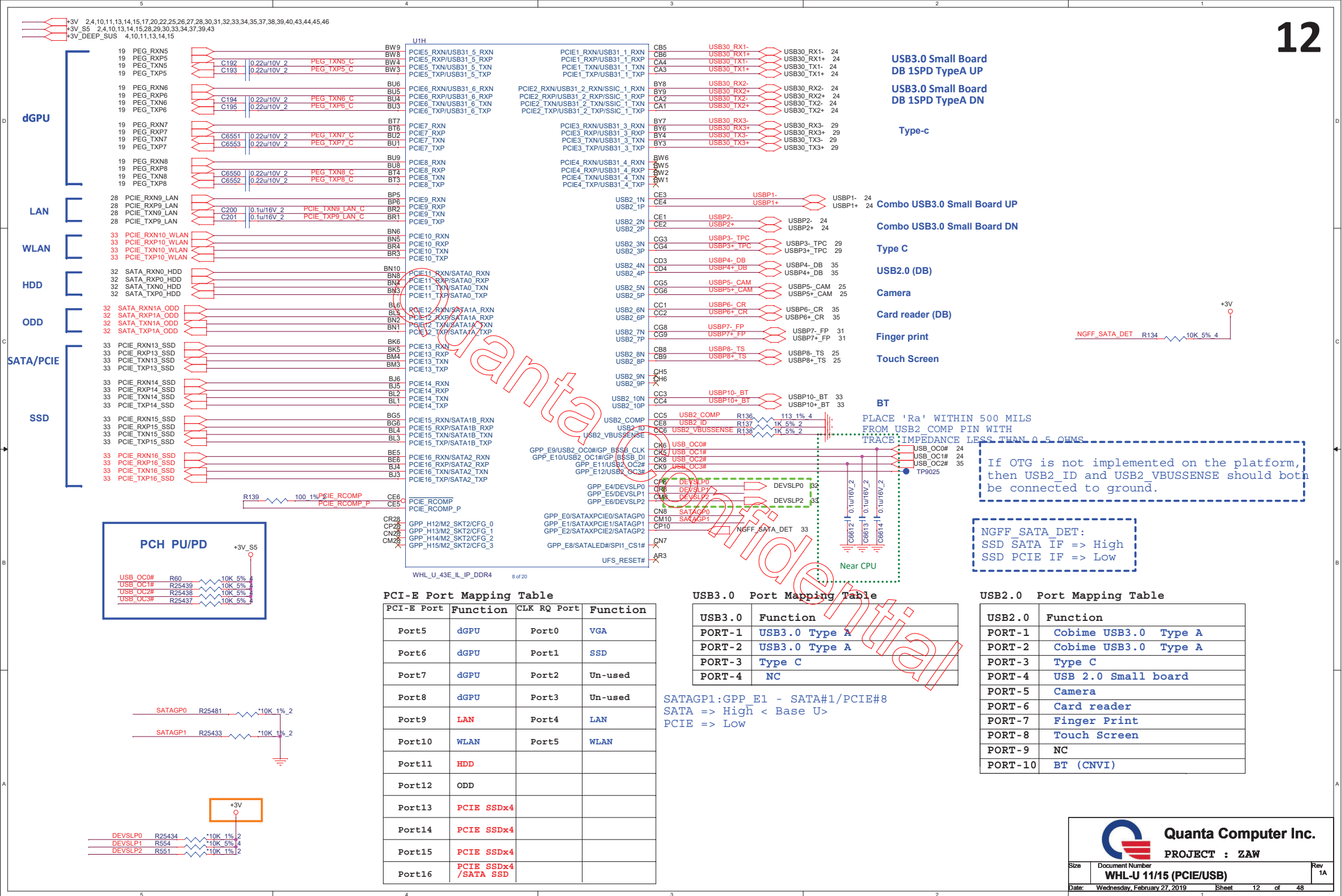
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

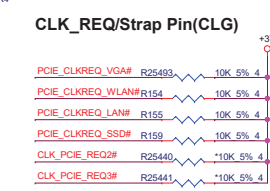
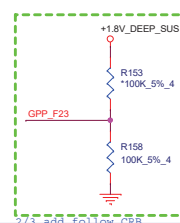
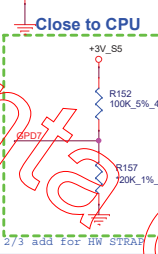
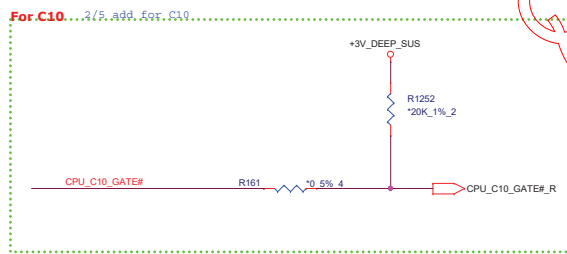
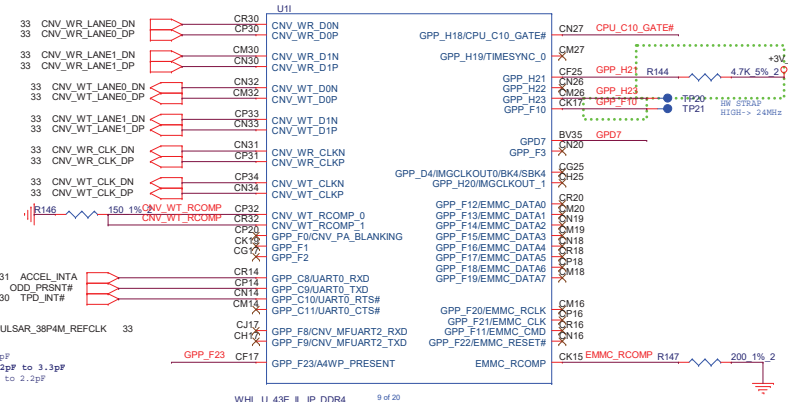
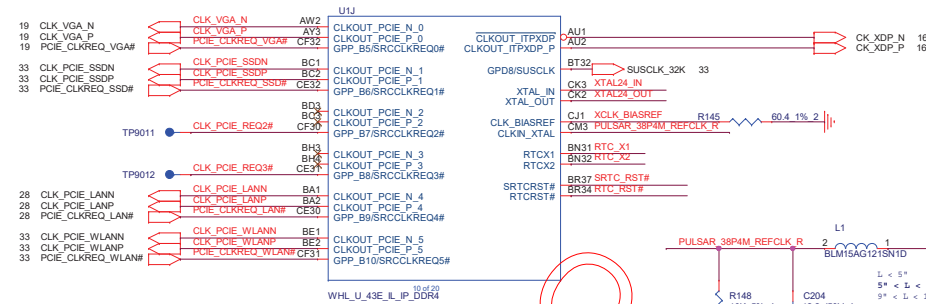
No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



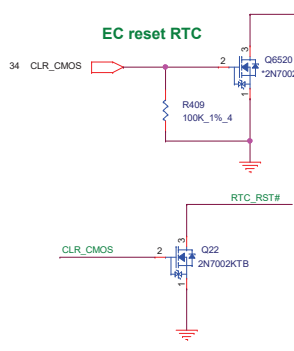
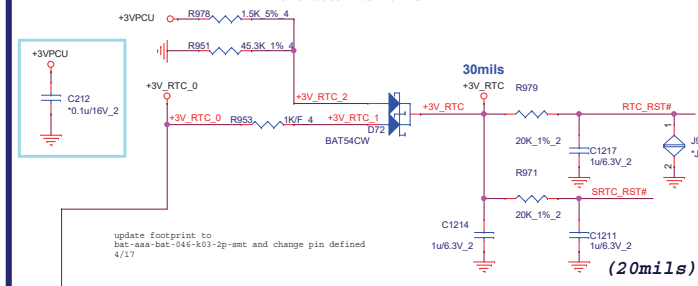
No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC

No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

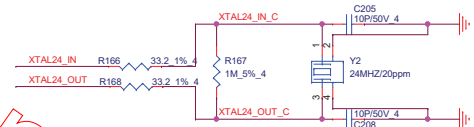


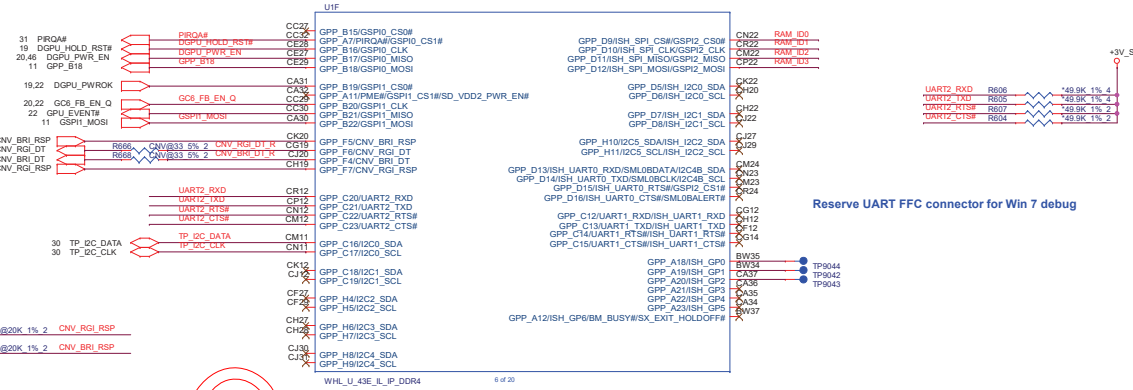


RTC Power trace width 20mils.

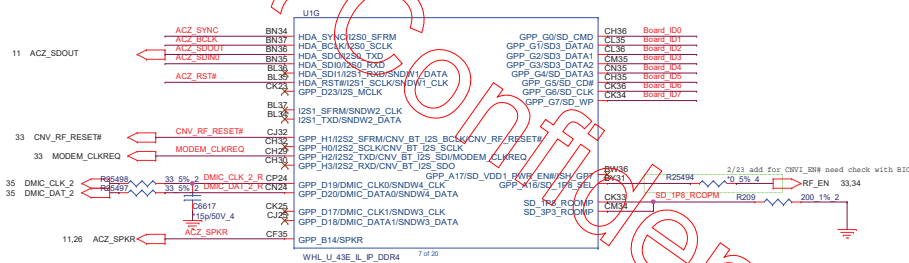
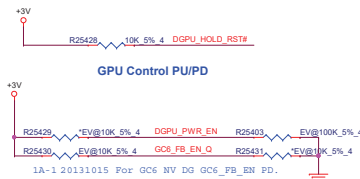
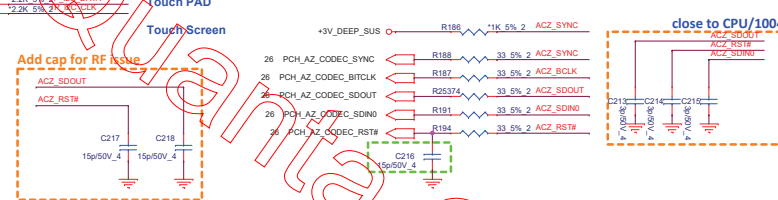


The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

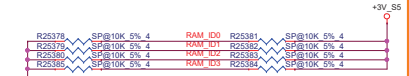




HDA Bus(CLG)

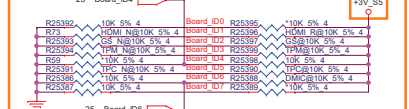


RAM ID



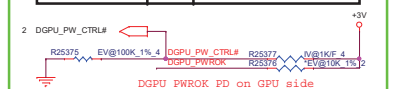
ID3	ID2	ID1	ID0	Vendor	Vendor PN	Quanta PN
0	0	0	0	Hynix 8Gb	HSAN8G6NCJR-KVC	AKDSQSGSTW13
0	0	0	1	Micron 8Gb	MT40A512M16LY-075:E	AKD5LZSTL24
0	0	1	0	Micron 8Gb	MT40A512M16TB-062EJ	AKDSQSGSTL23
1	1	1	1	With out on board memory		

Board ID

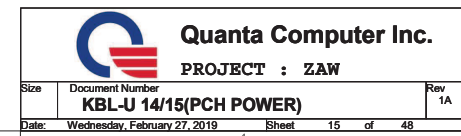


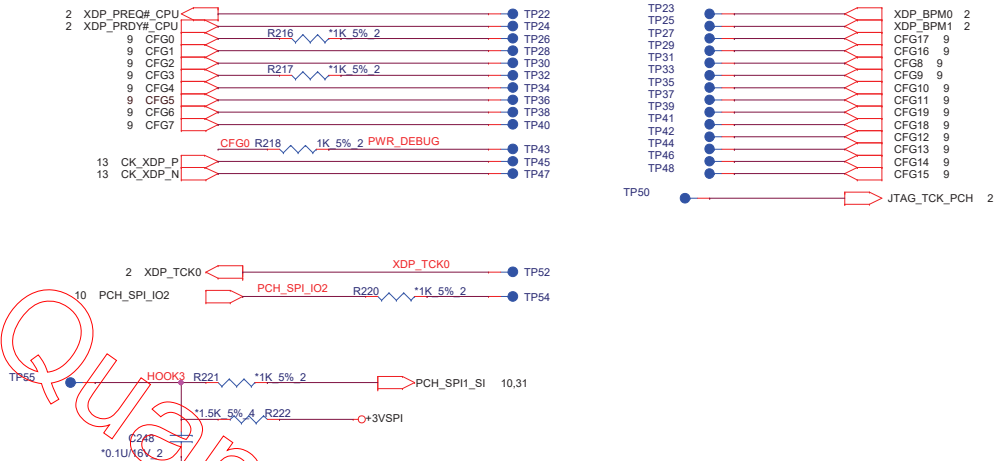
	Low	High
BOARD_ID0	Non eMMC	eMMC
BOARD_ID1	HDMI_N@	HDMI_R@
BOARD_ID2	Non G-sensor(GS_N@)	G-sensor(GS@)
BOARD_ID3	Non TPM(TPM_N@)	TPM(TPM@)
BOARD_ID4	Non Touch panel	Touch panel (Control by Cable)
BOARD_ID5	Non Type-C(TPC_N@)	Type-C(TPC@)
BOARD_ID6	Single MIC(Cable control)	Dual MIC (DMIC@)
BOARD_ID7	Reserved (Default)	Reserve

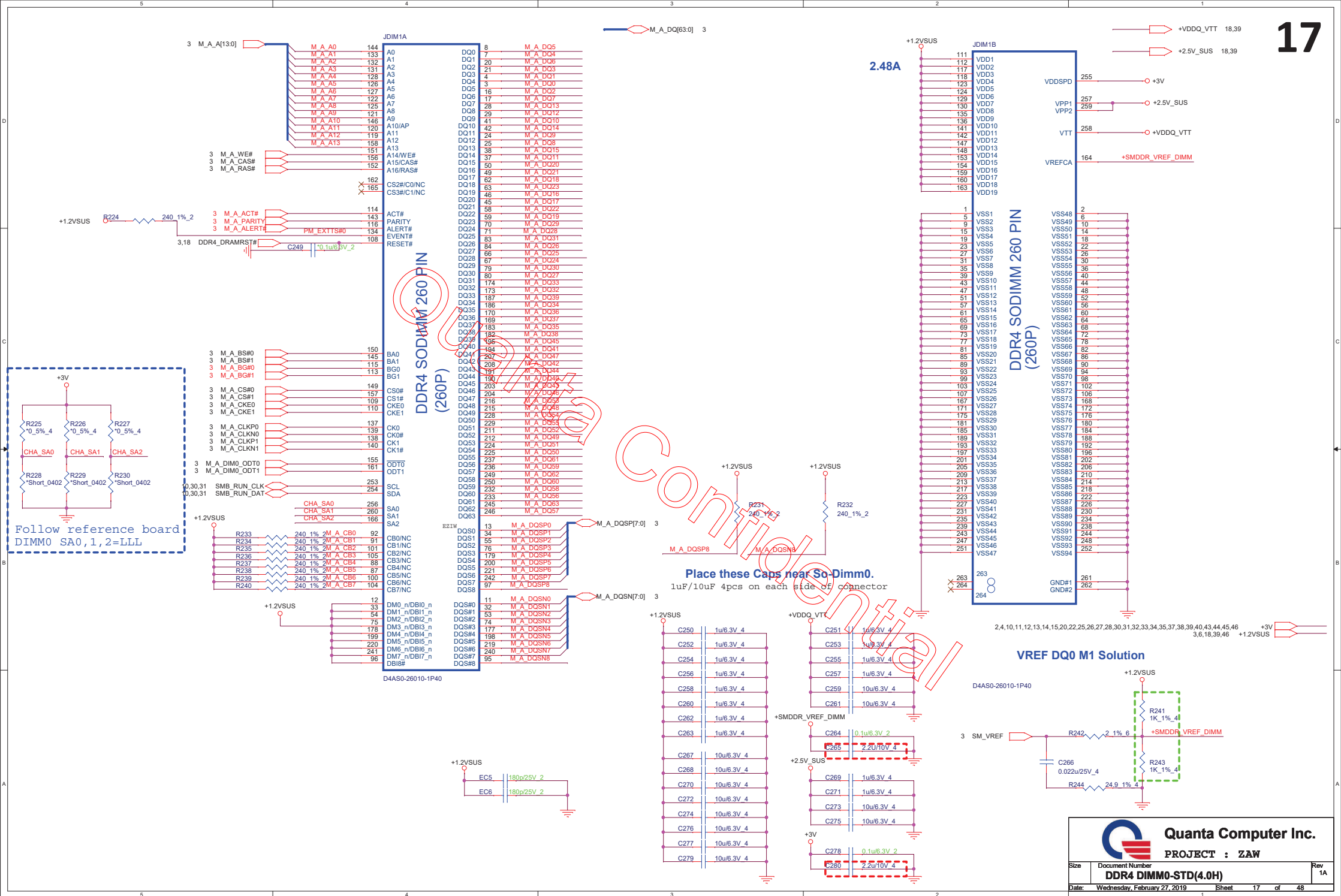
<i>DGPU_PW_CTRL#</i>	high	UMA Only
	low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

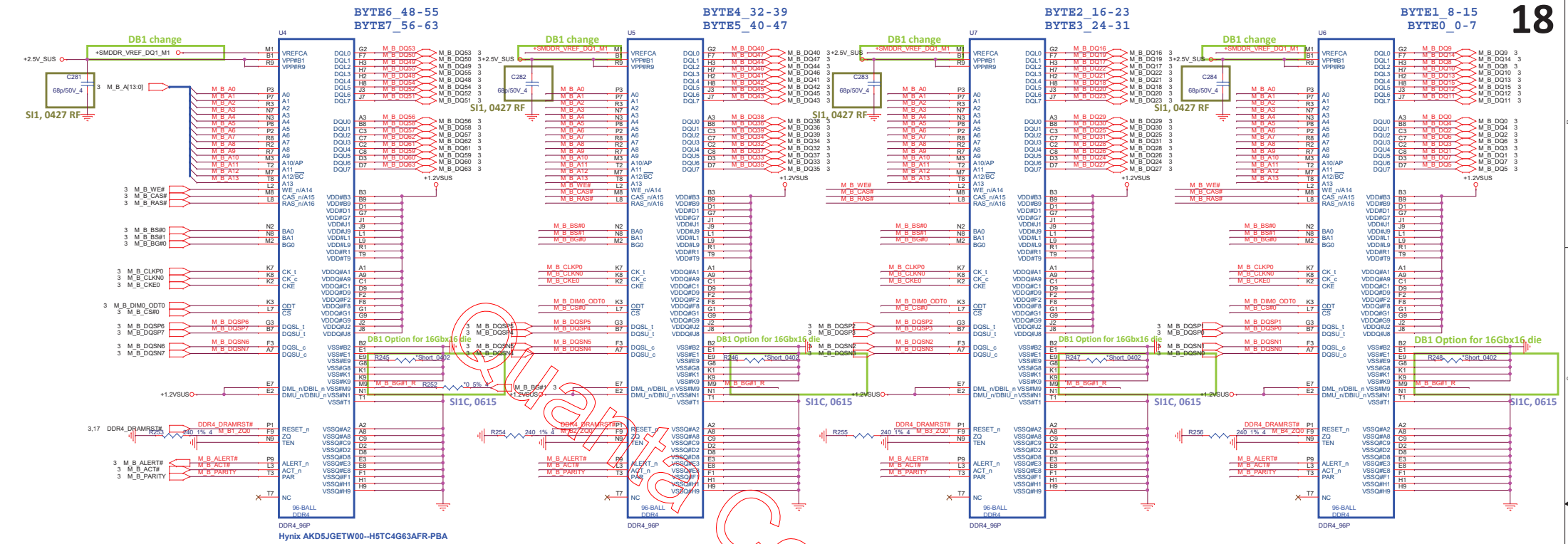


	DGPU_FW_CTRL#	VGA H/W Signal	Setup Menu	
UMA Only	1	UMA	Hidden	UMA boot
SG/Optimise	0	GPU	Hidden	GPU boot



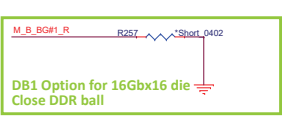




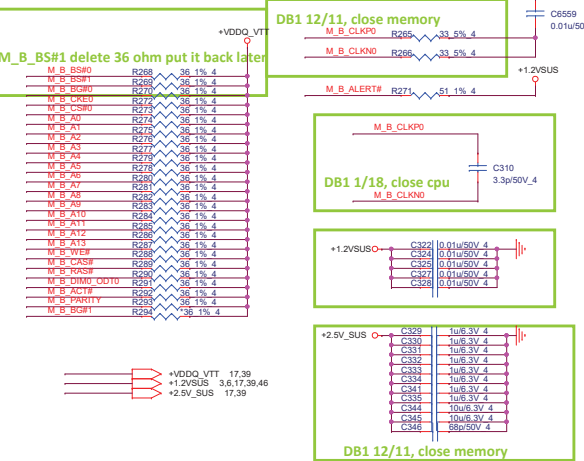


Vendor	P/N	Vendor	P/N
MIC 16G	AKDS5G0TL00	MT40A01G16BA-083E:A	
Elpida			
SAMSUNG			

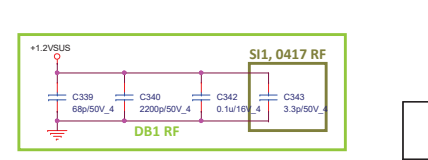
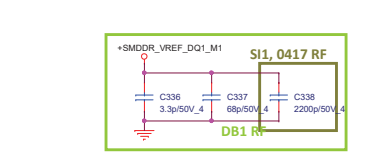
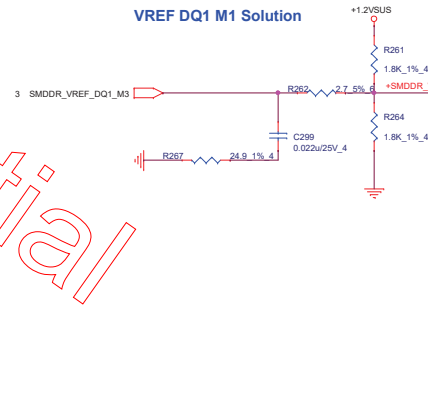
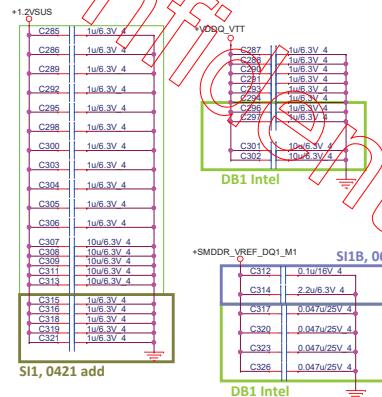
DDR4 mapping	SOP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS

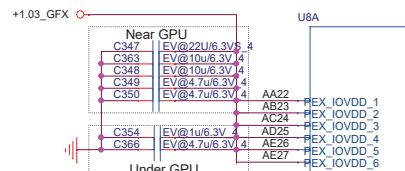
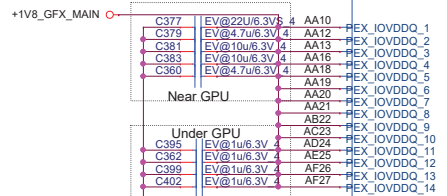


Memory 8G & Memory 16G TABLE			
	Memory 8G		Memory 16G
R278	0Q	CS000002JB38	240Q CS12402FB03
R279	0Q	CS000002JB38	240Q CS12402FB03
R280	0Q	CS000002JB38	240Q CS12402FB03
R281	0Q	CS000002JB38	240Q CS12402FB03
R282		UNINSTAL	INSTAL
R283		UNINSTAL	INSTAL
R284		UNINSTAL	INSTAL
R285		UNINSTAL	INSTAL
R290		UNINSTAL	UNINSTAL
R291		UNINSTAL	UNINSTAL
R292		UNINSTAL	UNINSTAL
R293		UNINSTAL	UNINSTAL

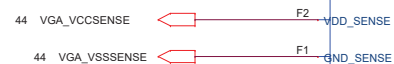
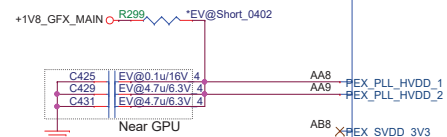


Place these Caps near Channel B
1uF/10uF 4pcs on each side of connector

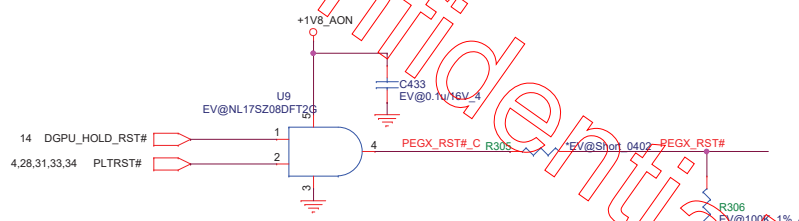
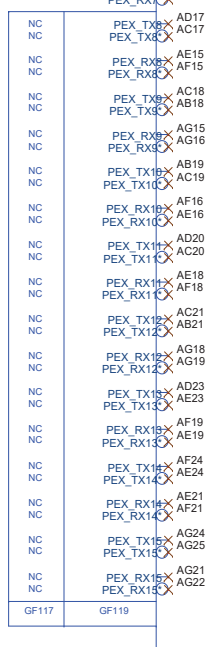
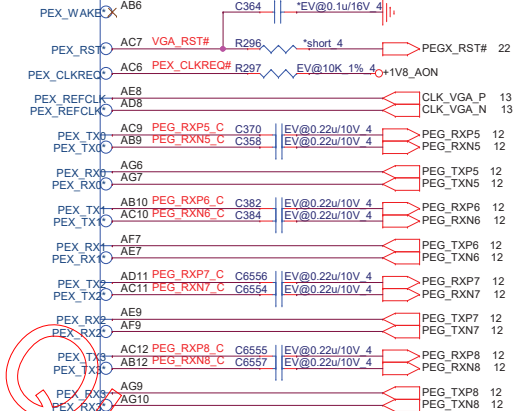
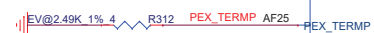



$$\text{PEX IOVDD} + \text{PEX IOVDDQ} = 1.042\text{A}$$


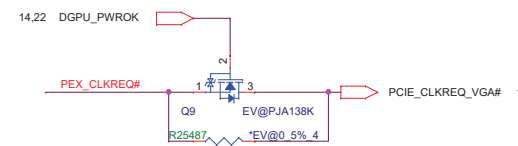
PEX_PLL_HVDD +
PEX_SVDD 3V3 = 143mA



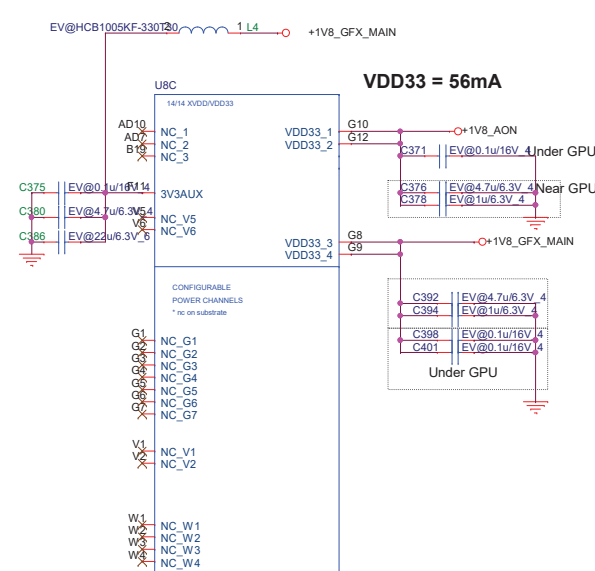
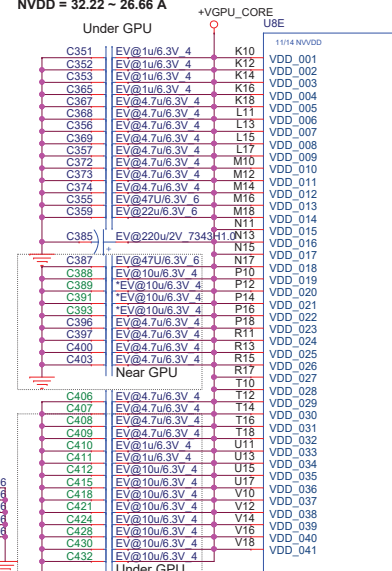
PEX_PLLVDD = 130mA



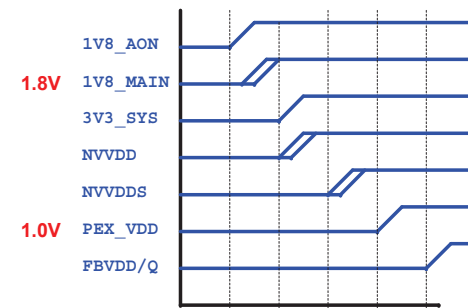
net PCIE CLKREQ VGA# and PU:10K both remove in CPU side



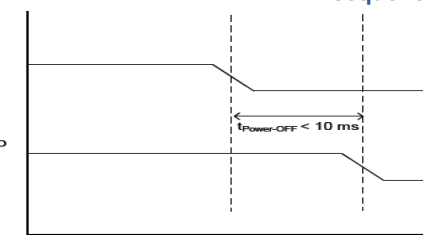
NVDD = 32.22 ~ 26.66 A



Power up sequence



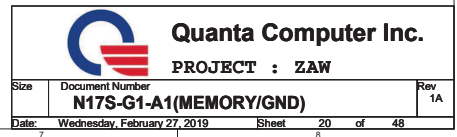
Power down sequence

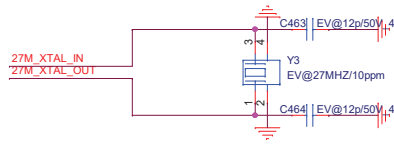


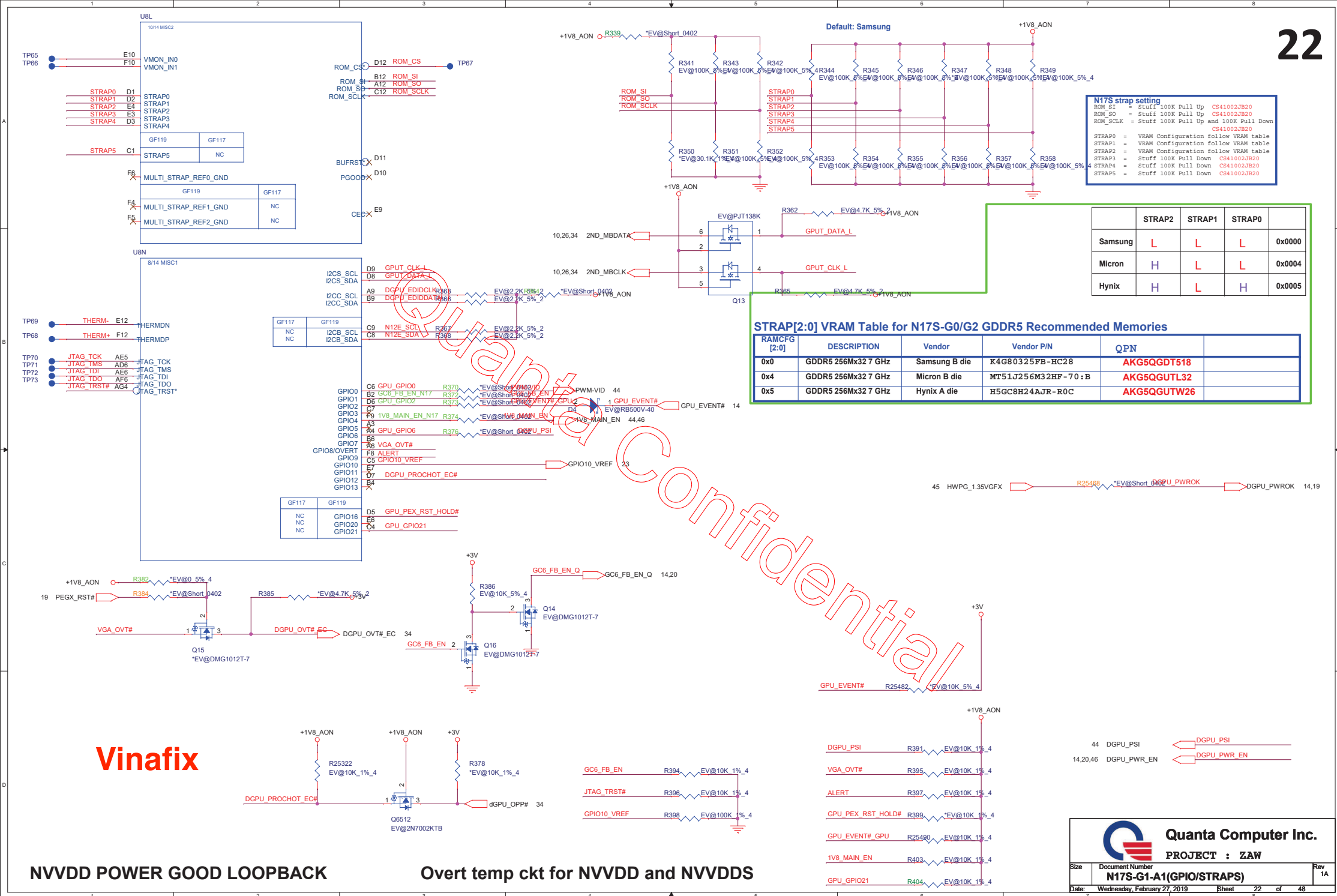
Quanta Computer Inc.

PROJECT : ZAW

Size	Document Number N17S-G1-A1(PCIE I/F)/NVDD	Rev 1A
Date:	Wednesday, February 27, 2019	Sheet 19 of 48







MF=0 Non-mirrored

Channel 0 MF=0 Non-mirrored
<0-31>

CHANNEL A: 2G/4G GDDR5

Channel 0 MF=0 Non-mirrored
<32-63>

23

QD24~31

QD16~23

QD8~15

QD0~7

QD40~47

QD32~39

QD56~63

QD48~55

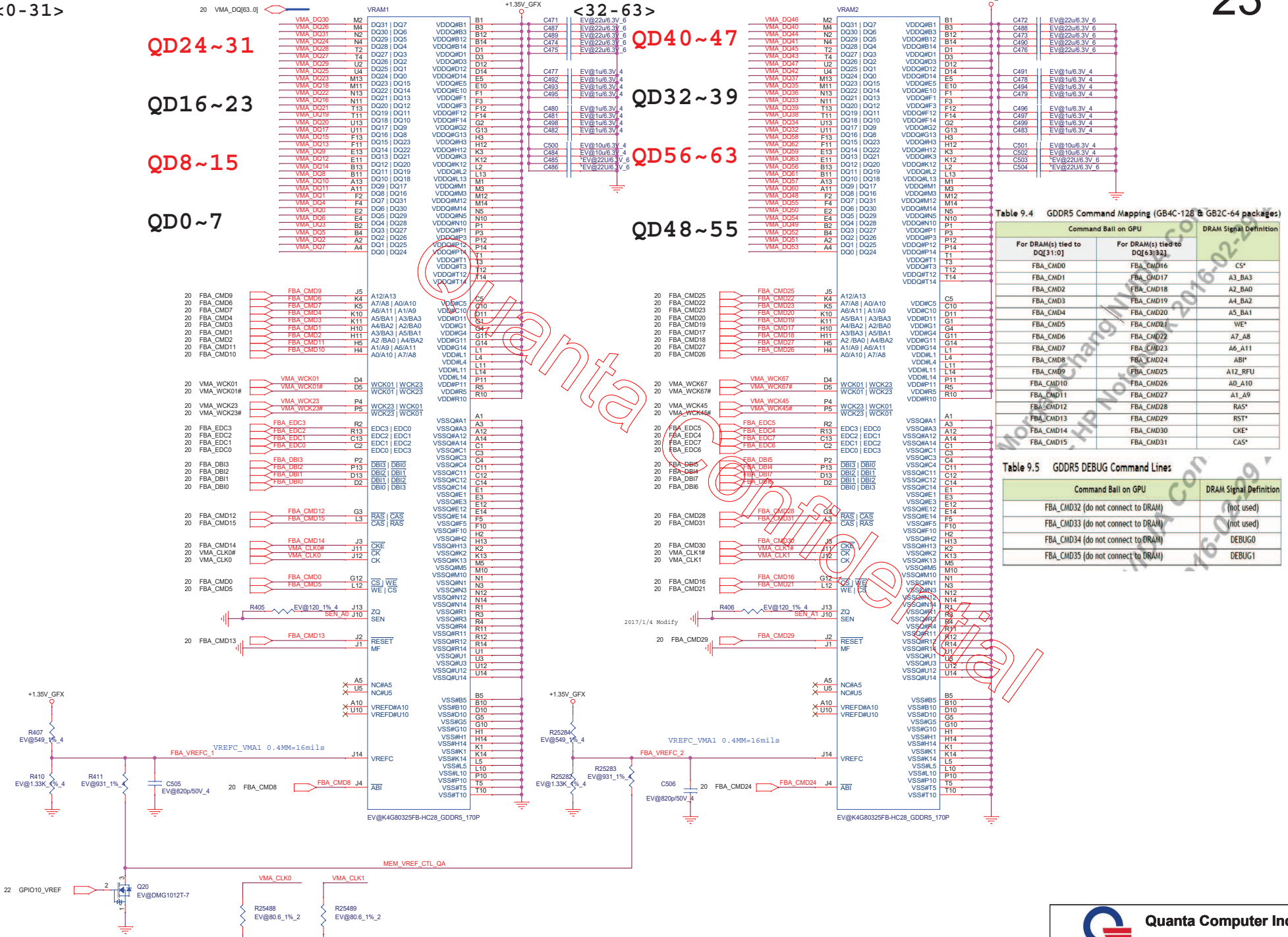


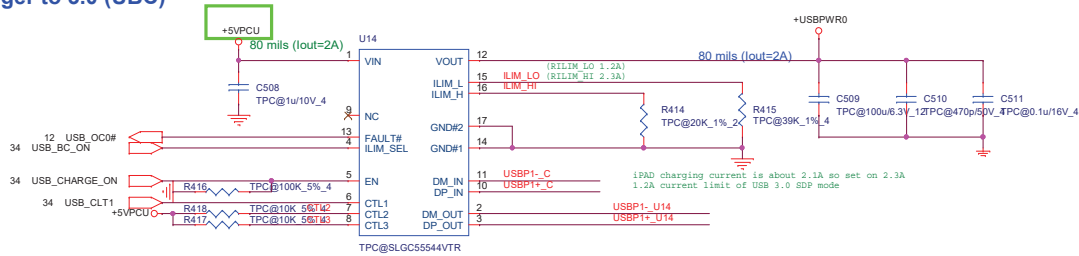
Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition	
For DRAM(s) tied to DQ[63:32]	For DRAM(s) tied to DQ[63:32]		
FBA_CMD0	FBA_CMD16	CS*	
FBA_CMD1	FBA_CMD17	A3_BA3	
FBA_CMD2	FBA_CMD18	A2_BA0	
FBA_CMD3	FBA_CMD19	A4_BA2	
FBA_CMD4	FBA_CMD20	A5_BA1	
FBA_CMD5	FBA_CMD21	WE*	
FBA_CMD6	FBA_CMD22	A7_A8	
FBA_CMD7	FBA_CMD23	A6_A11	
FBA_CMD8	FBA_CMD24	AB1*	
FBA_CMD9	FBA_CMD25	A12_RFU	
FBA_CMD10	FBA_CMD26	A0_A10	
FBA_CMD11	FBA_CMD27	A1_A9	
FBA_CMD12	FBA_CMD28	RAS*	
FBA_CMD13	FBA_CMD29	RST*	
FBA_CMD14	FBA_CMD30	CKE*	
FBA_CMD15	FBA_CMD31	CAS*	

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

USB Charger to 3.0 (UBC)

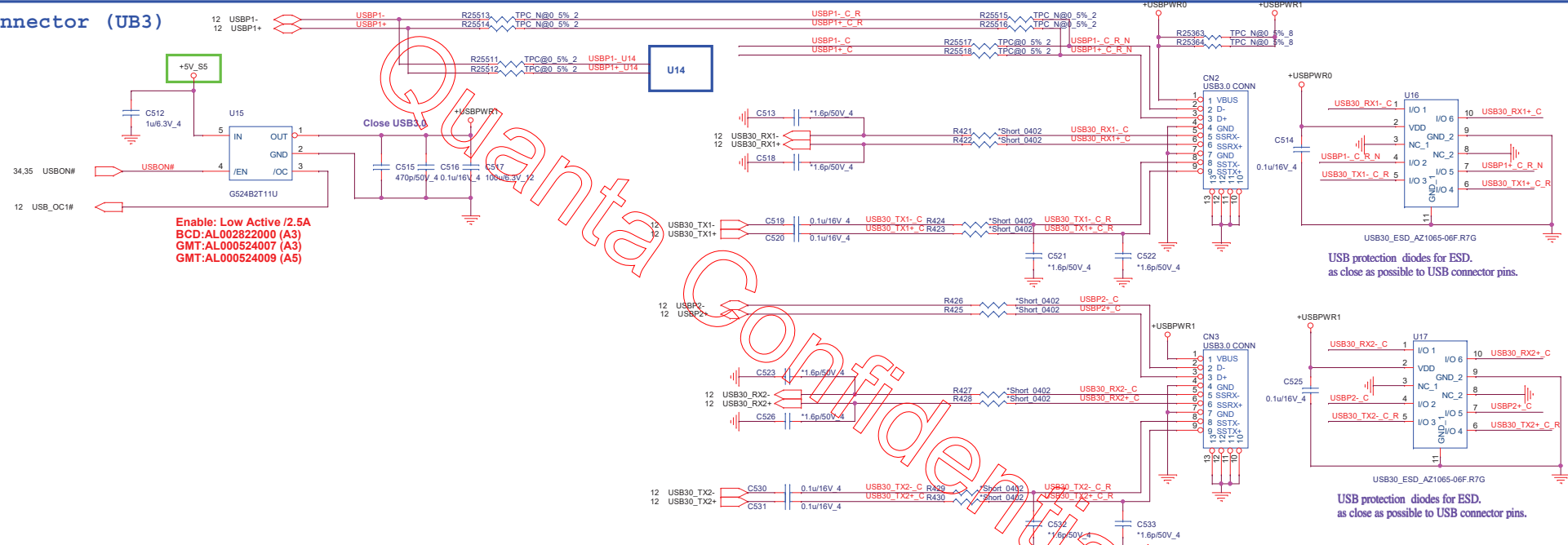


	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

TI:AL002544001 (TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1) $I_{OS_typ}(mA) = 50,250 / \{RILIM_XX(k\Omega) + 0.1\}$
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

USB 3.0 Connector (UB3)



Enable: Low Active /2.5A
BCD:AL002822000 (A3)
GMT:AL000524007 (A3)
GMT:AL000524009 (A5)

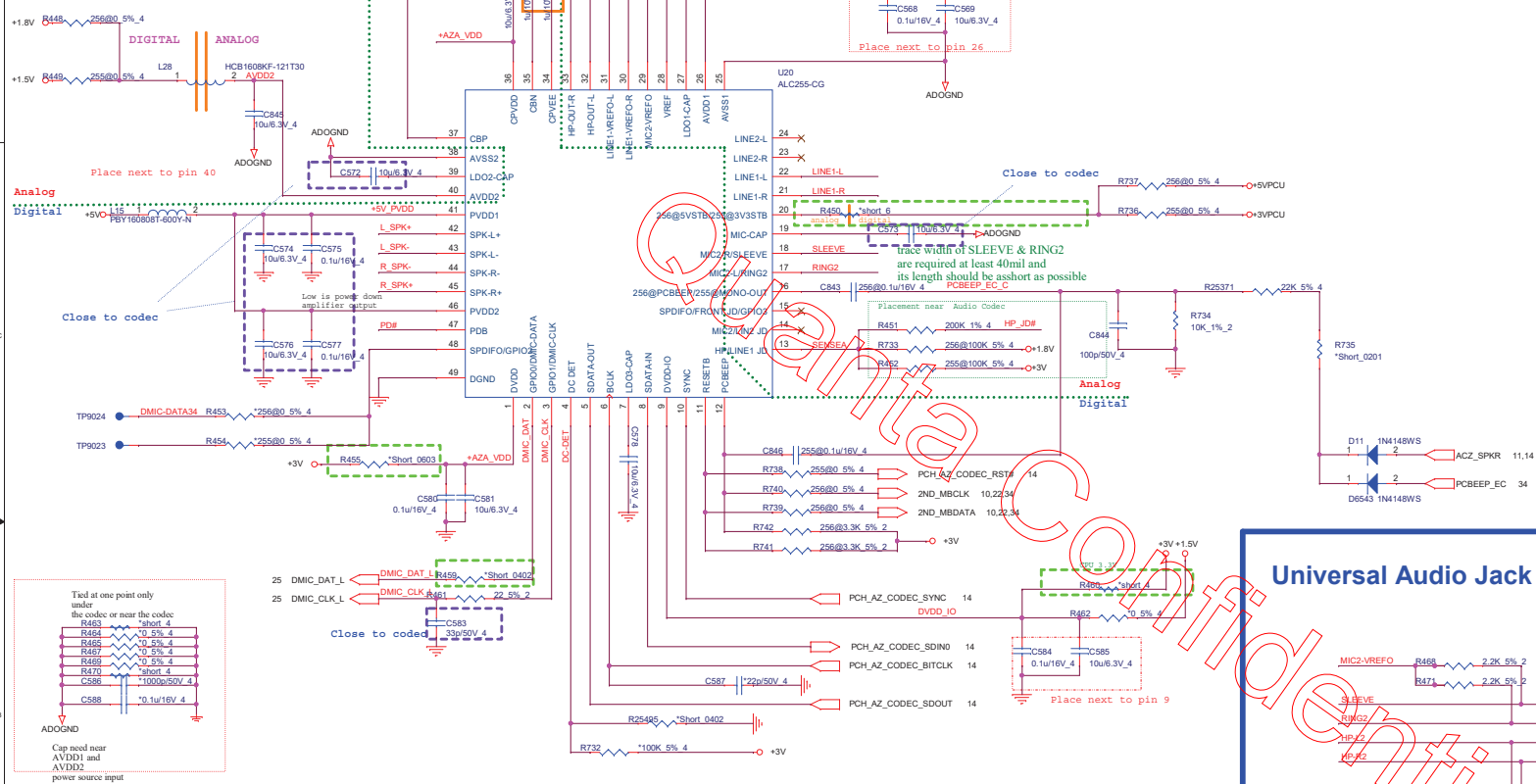
USB protection diodes for ESD.
as close as possible to USB connector pins.

USB protection diodes for ESD.
as close as possible to USB connector pins.

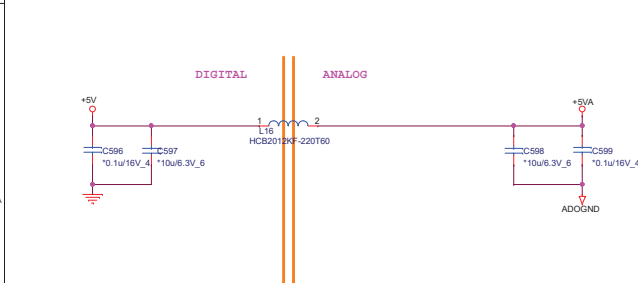
CAP close to different CONN

Codec(ADO)

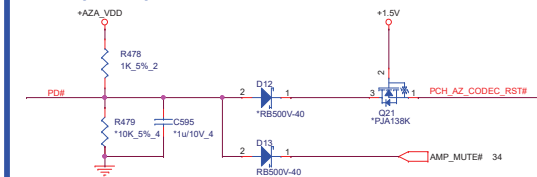
Codec PWR 1.5V(ADO)



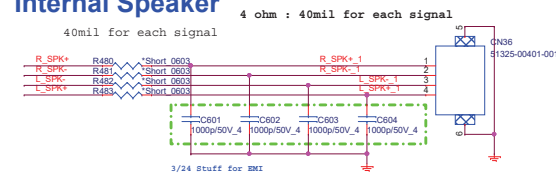
Codec PWR 5V(ADO)



Mute(ADO)

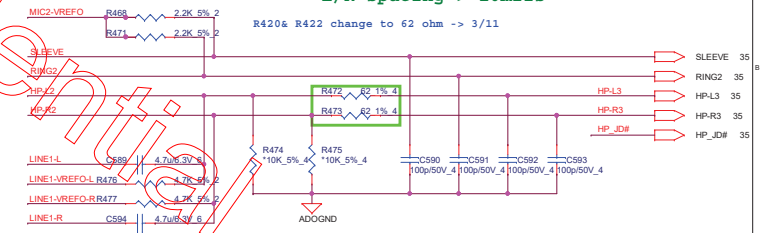


Internal Speaker



Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

SLEEVE/RING2 trace > 40mils
HP/LINE trace > 10mils
L/R spacing > 10mils



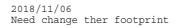
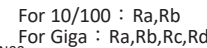
Quanta Computer Inc.

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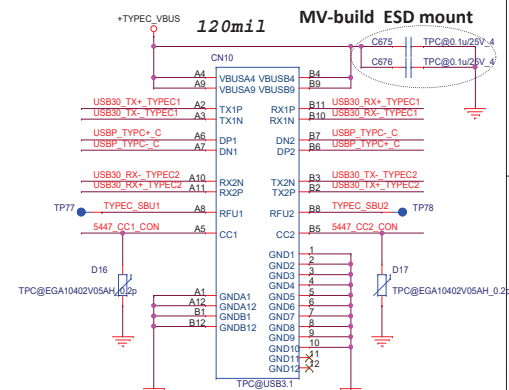
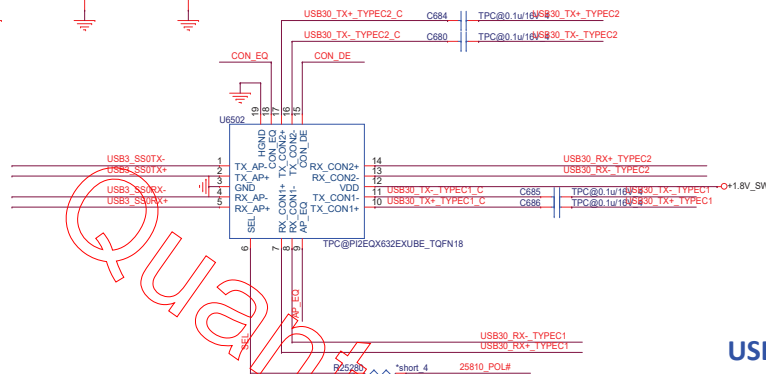
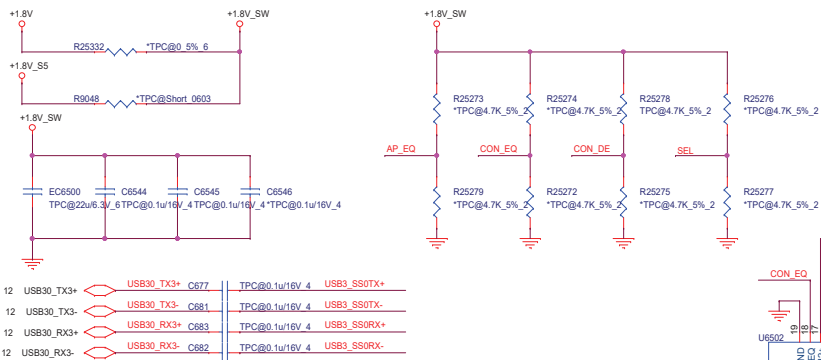
Size Document Number
Audio Codec/HP/SPK/Hole
Date: Wednesday, February 27, 2019 Sheet 26 of 48

* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG
close to each VDD10 pin-- 3, 22, 8 , 30

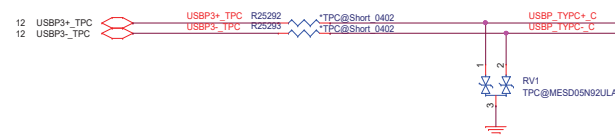
* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG
close to each VDD10 pin-- 22(reserved)



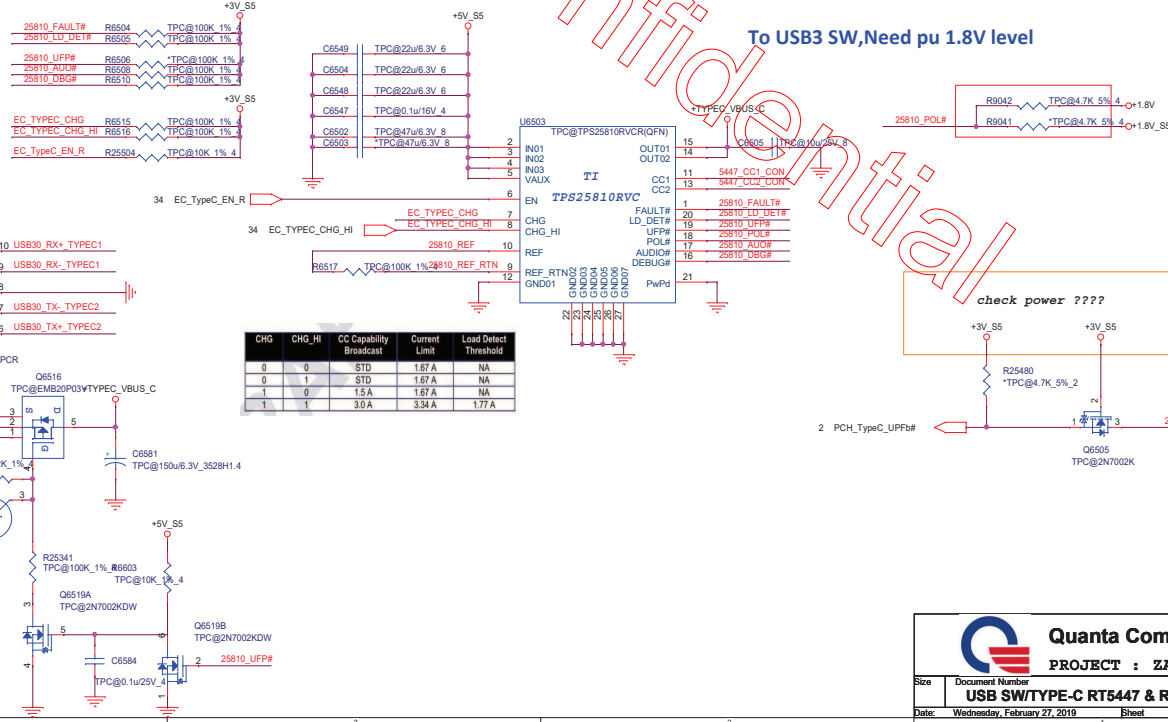
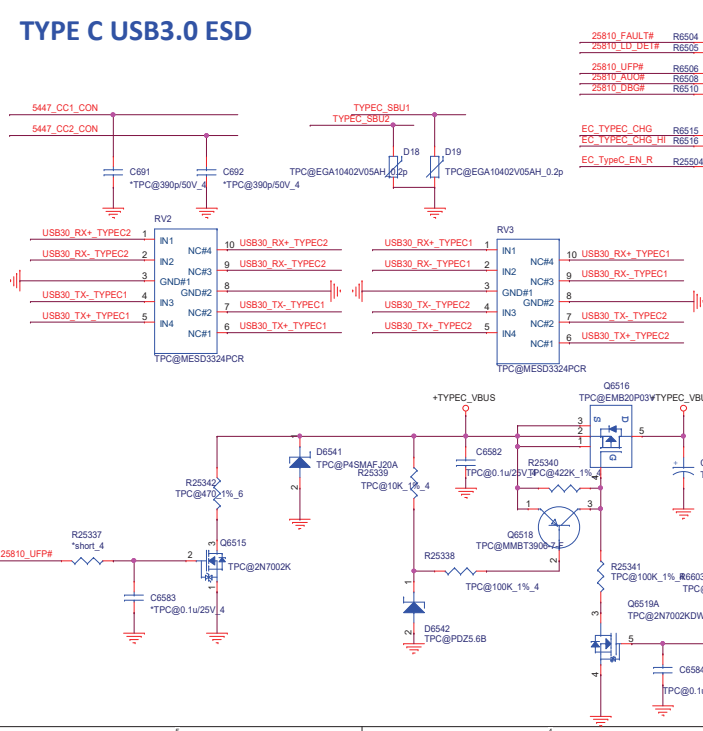
TYPE C and MUX PI2EQX632EXUBE



USB2.0



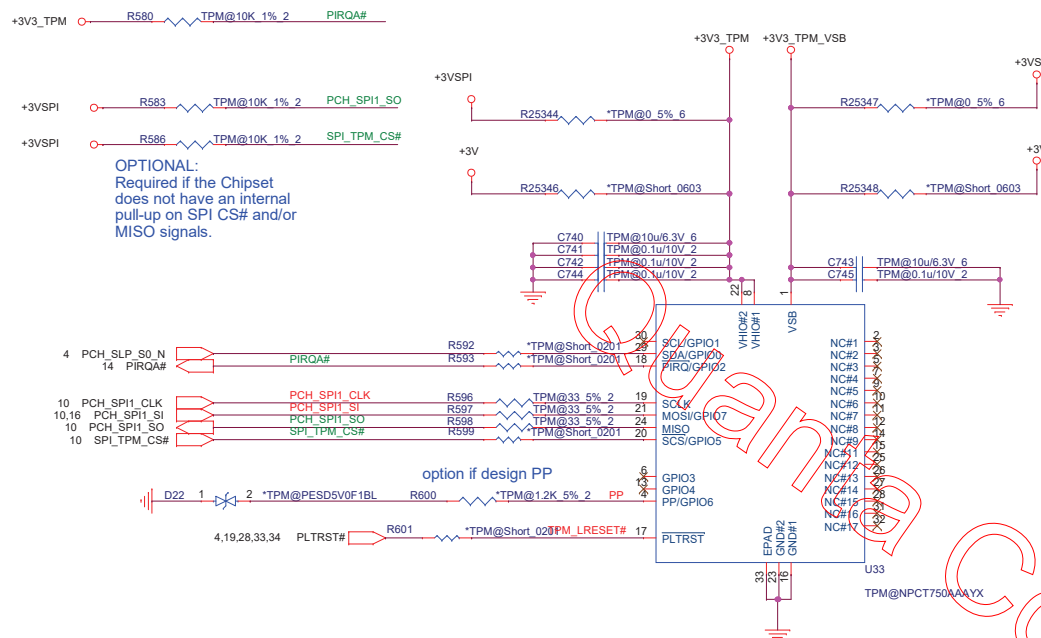
TYPE C USB3.0 ESD



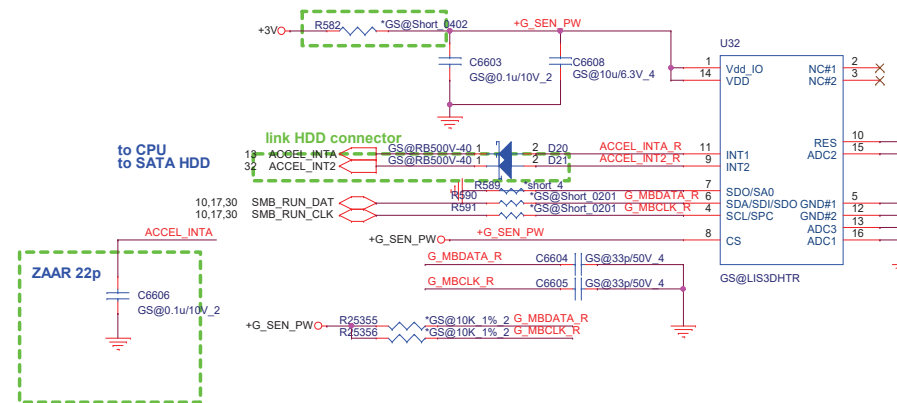
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

check power ???

TPM NPCT750

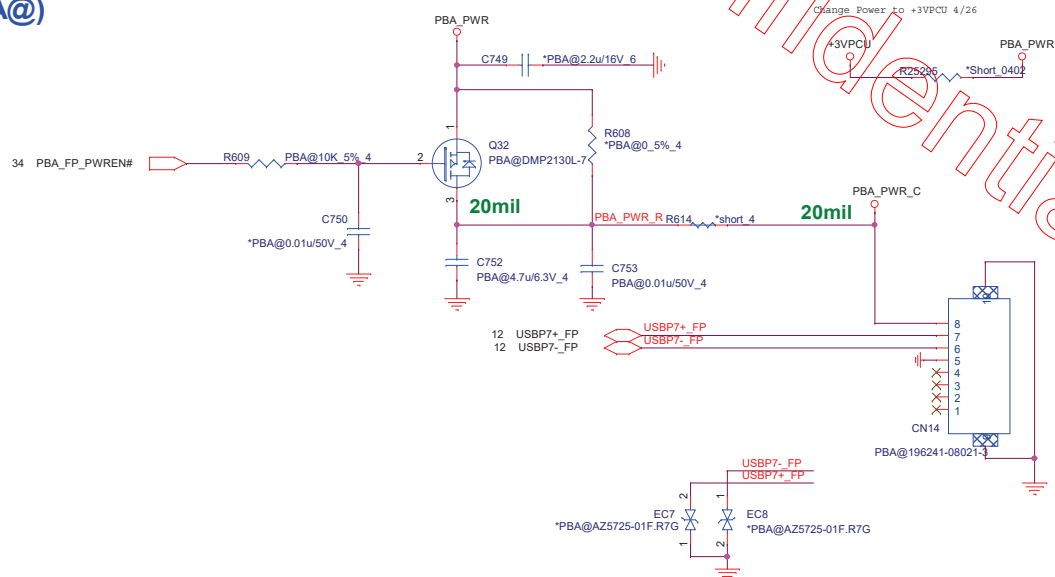


G-sensor (GS@)



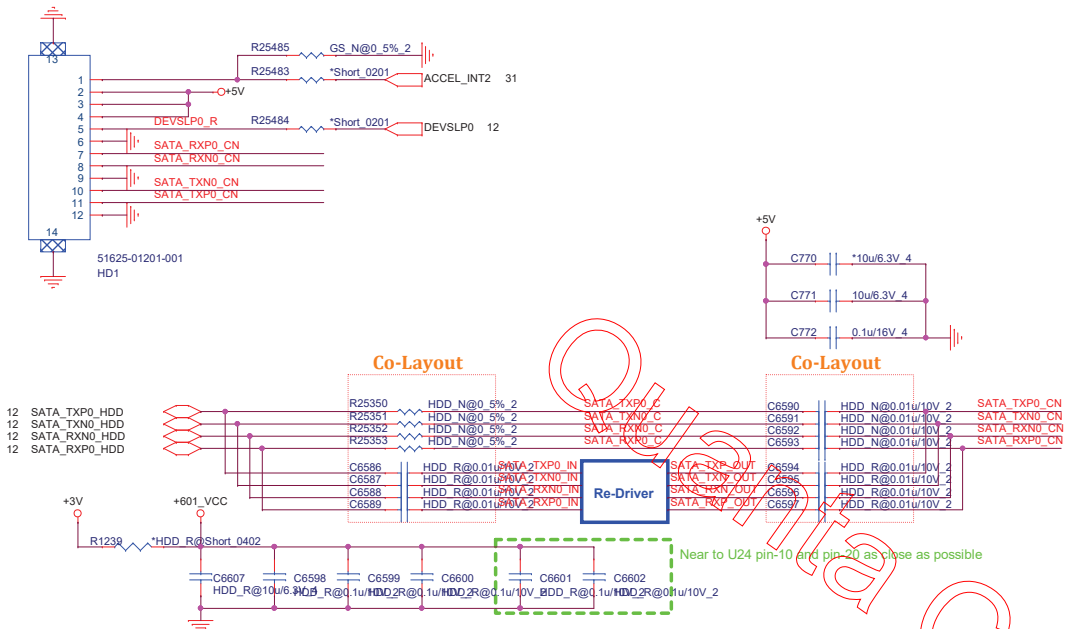
Vinafix

PBA (PBA@)



SATA HDD & LED

24,29,35,37,39,40,41,42,44,45,46 +5V_S5
25,26,27,30,37,43 +5V
2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,33,34,35,37,38,39,40,43,44,45,46 +3V
2,4,10,12,13,14,15,28,29,30,33,34,37,39,43 +3V_S5
9,15,38 +1.05V_DEEP_SUS



SATA HDD Re-driver

BQ2	H - 14dB
X - 0dB	
L - 7dB	

BQ1	H - 14dB
X - 0dB	
L - 7dB	

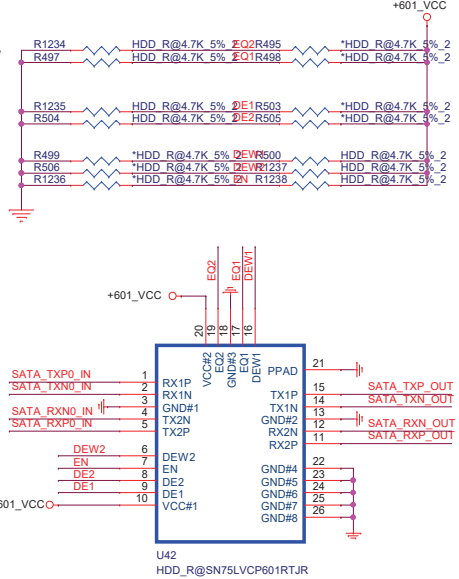
DEW1	H - Long Duration
X - NC (Long)	
L - Short Duration	

DE1	H - -2dB
X - -4dB	
L - 0dB	

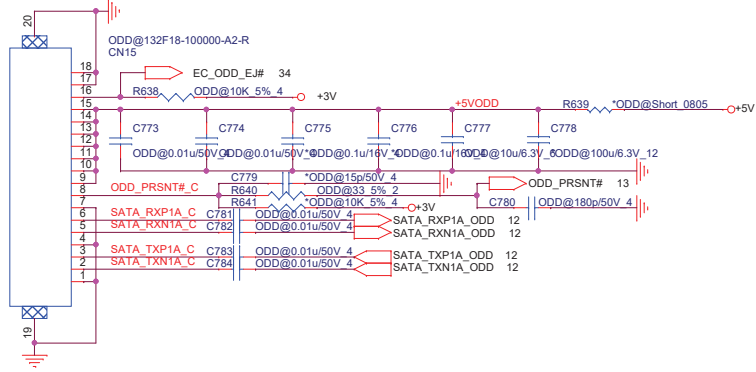
DE2	H - -2dB
X - -4dB	
L - 0dB	

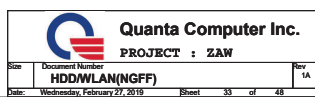
DEW2	H - Long Duration
X - NC (Long)	
L - Short Duration	

SW7 - EN	
H - Enabled	
L - Standby Mode	

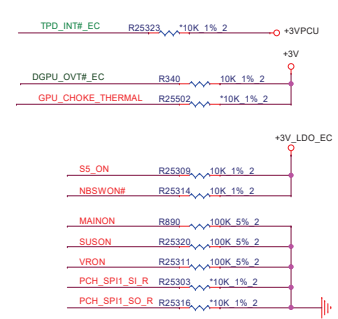
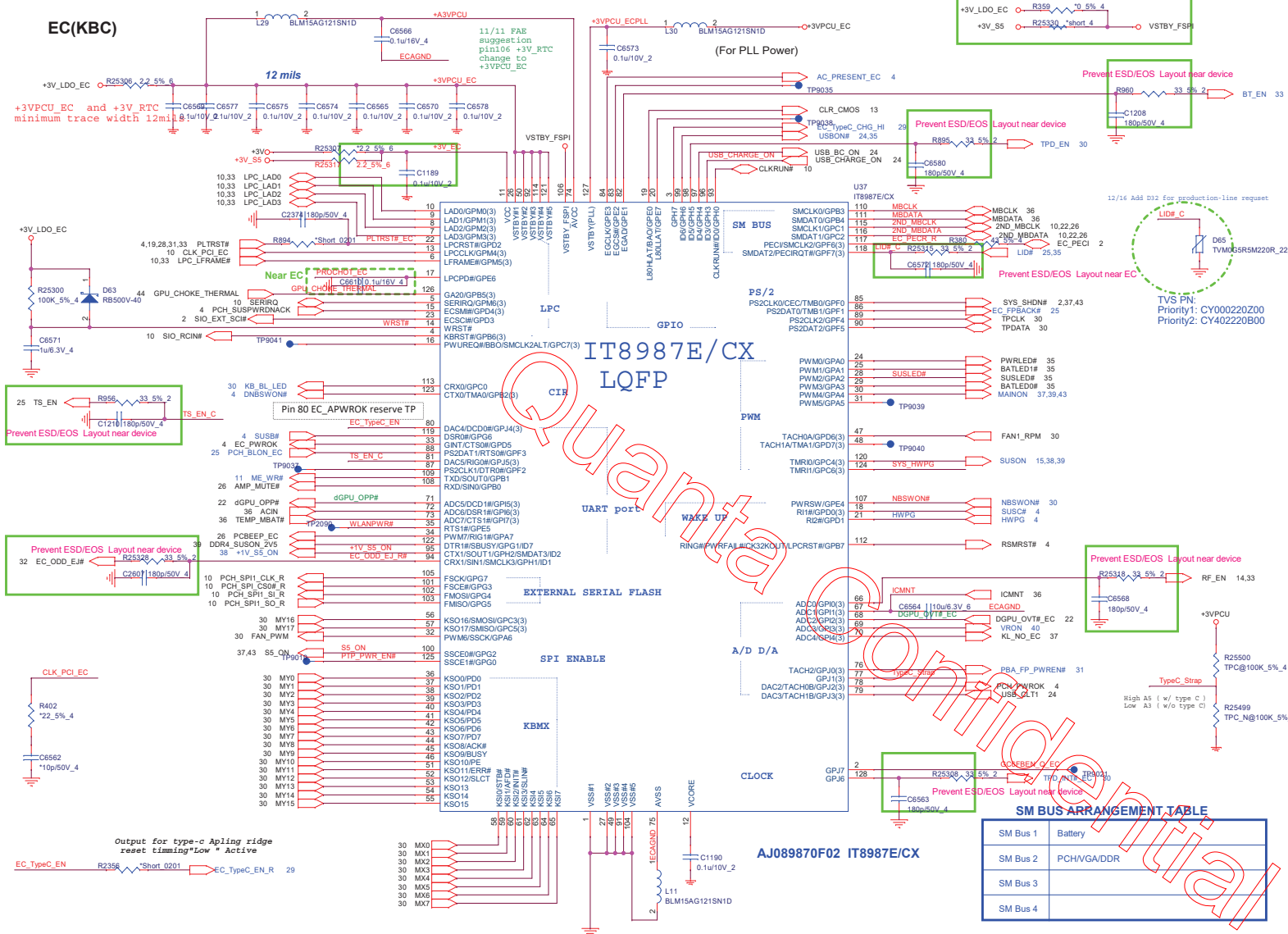


SATA ODD (ODD@)

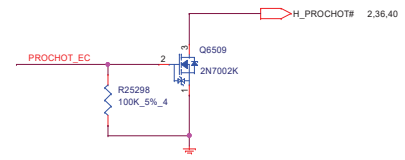
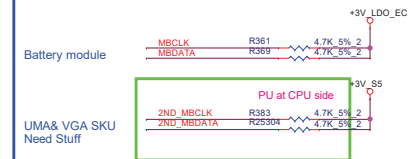




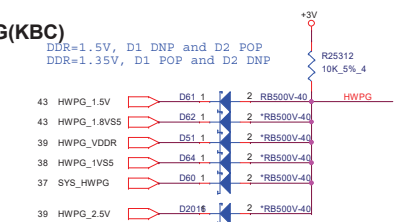
EC(KBC)



SM BUS PU(KBC)

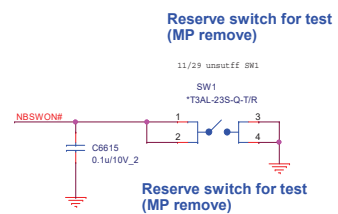
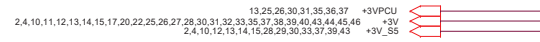
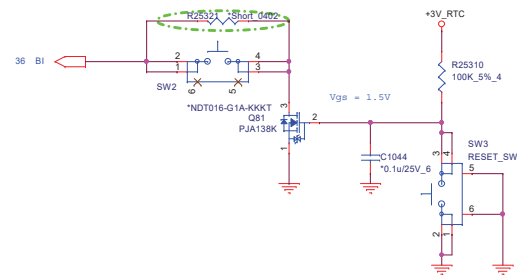


HWPG(KBC)



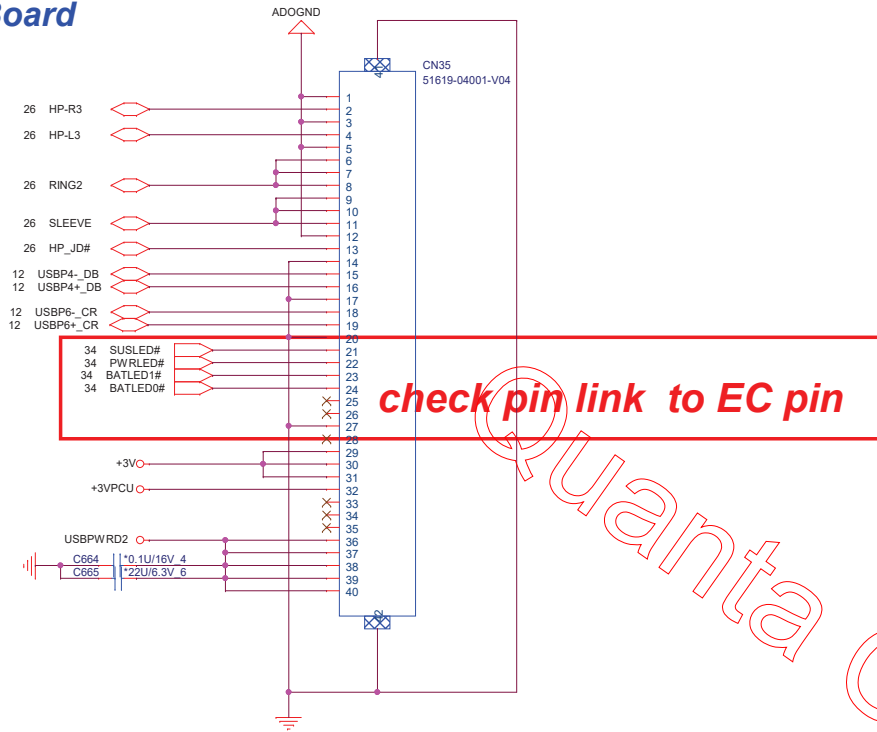
Reset SW (FSW)

Battery Detect Switch

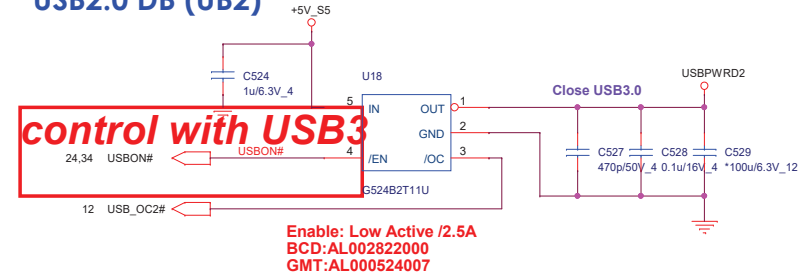


Vinafix

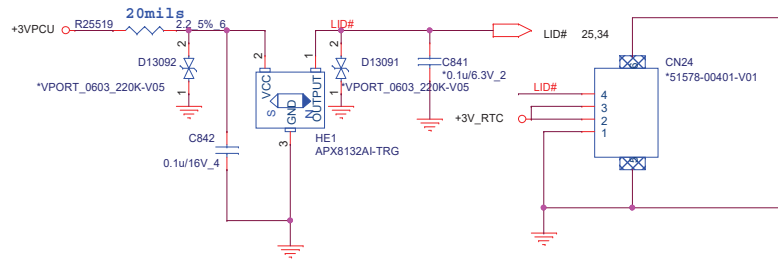
USB Board



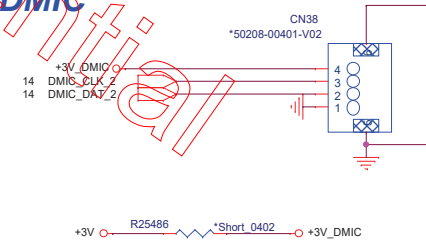
USB2.0 DB (UB2)



Hall Sensor



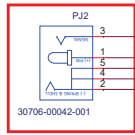
DMIC



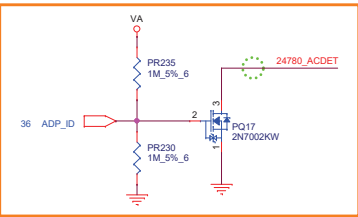
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Double Check ADP-IN Connector with ME

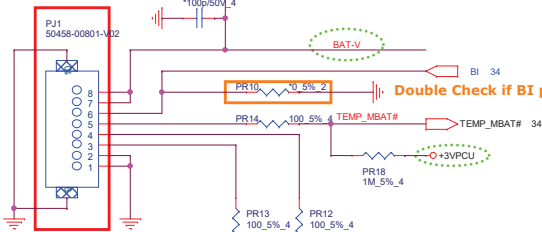


PR23	UMA	DIS
41.2K Ohm CS34122FB19	33.2K Ohm CS33322FB13	
78W	95W	



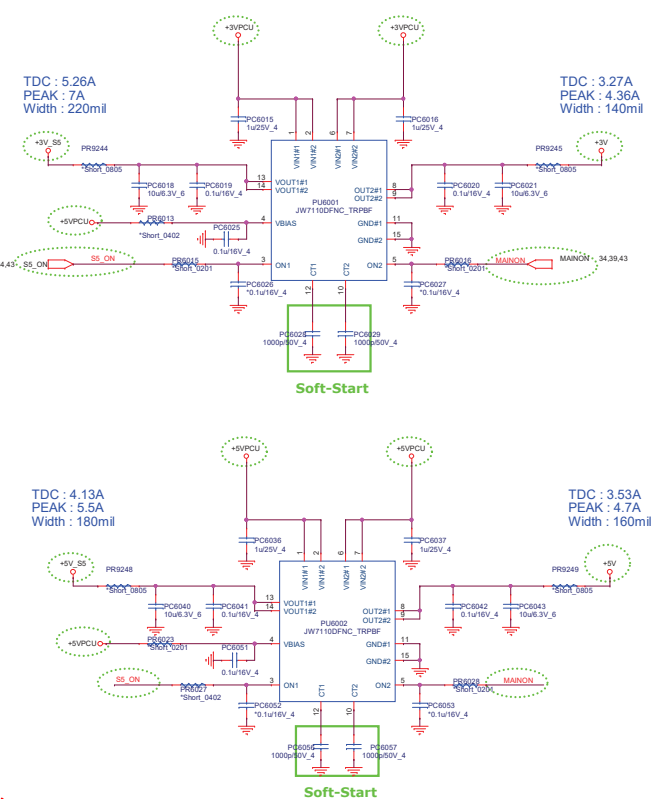
- (1) BQ24780S : 1 μ A/W (default)
(2) RT3602AJ : PSYS = 3.2V

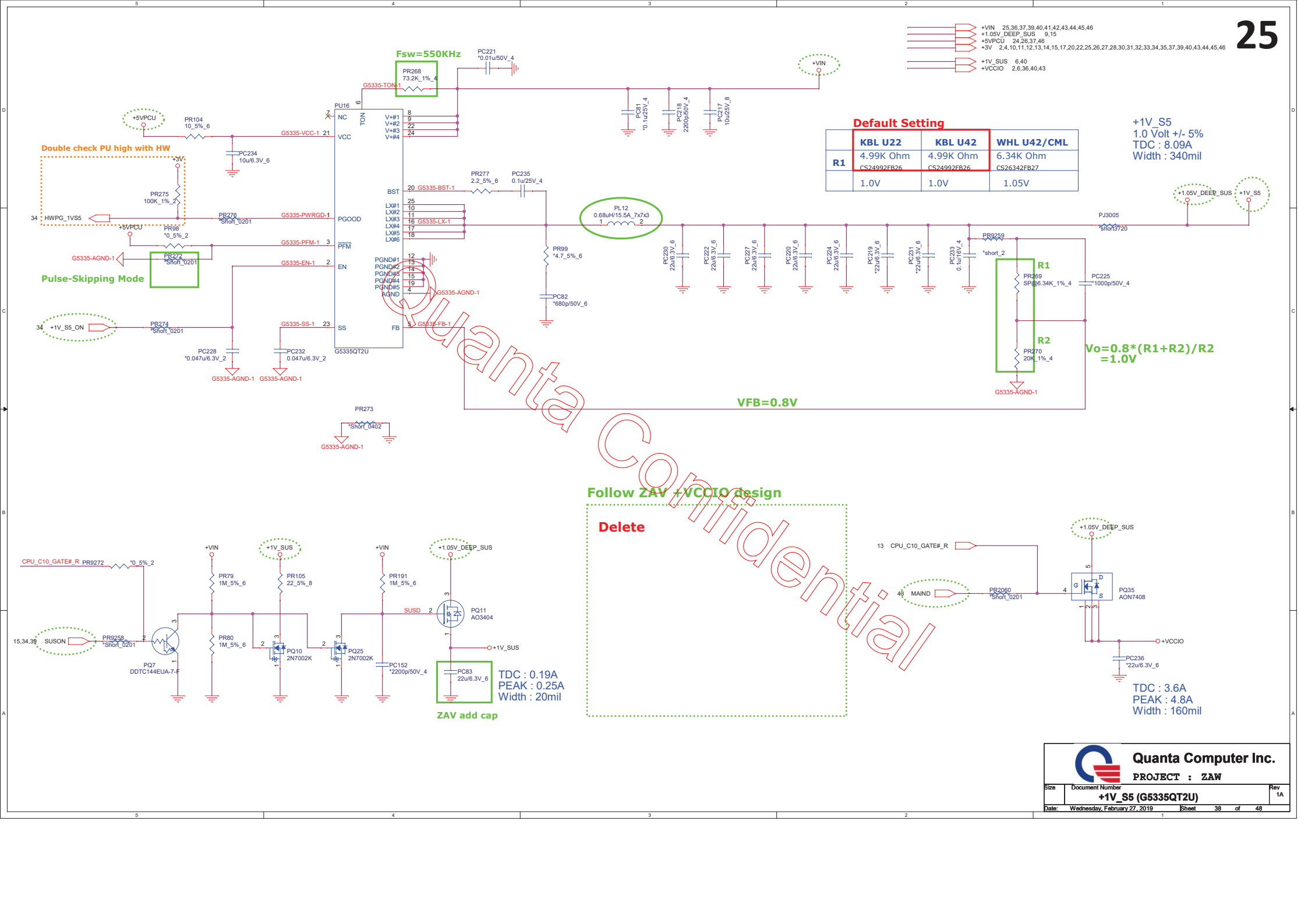
CS34122FB19 RES CHIP 41.2K 1/16W +1% (0402) For 78W
CS33322FB13 RES CHIP 33.2K 1/16W +1% (0402) For 95W
CS32742FB14 RES CHIP 27.4K 1/16W +1% (0402) For 116W

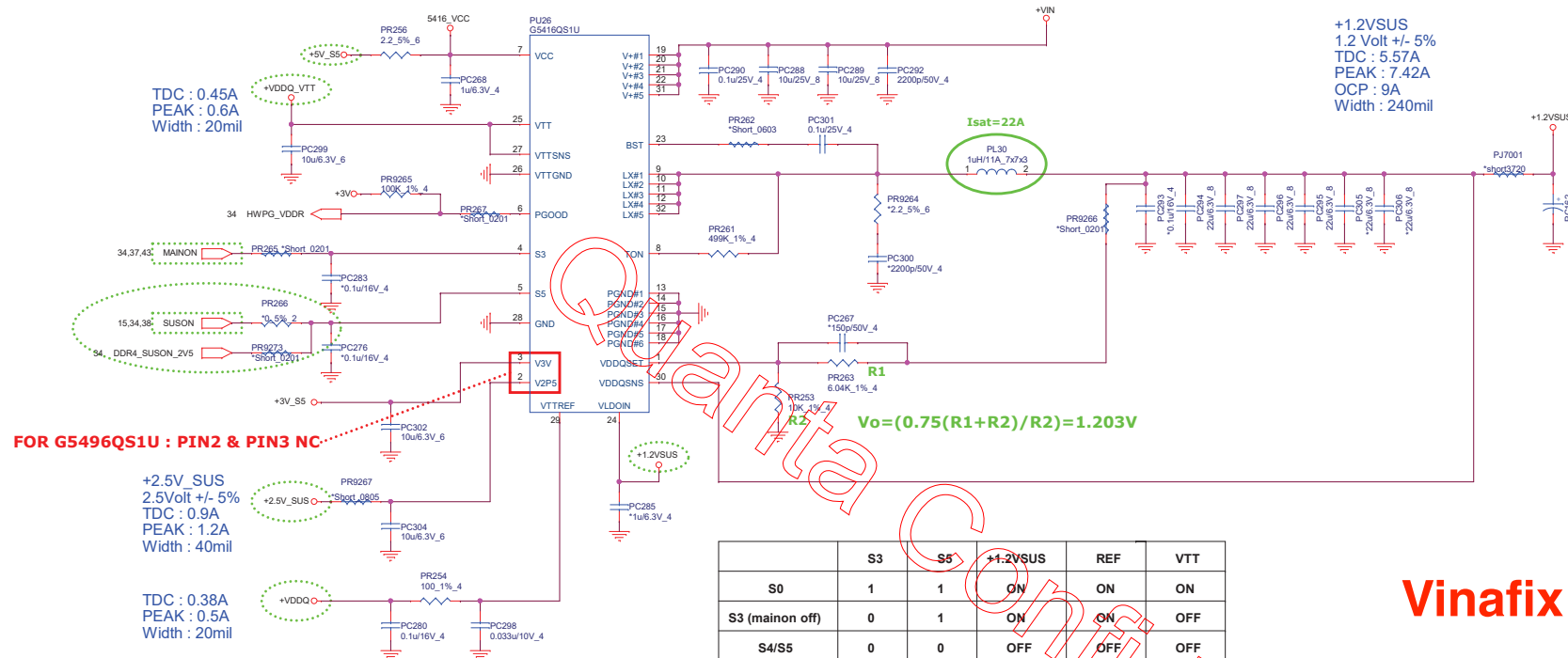


Double Check BATT Connector with ME

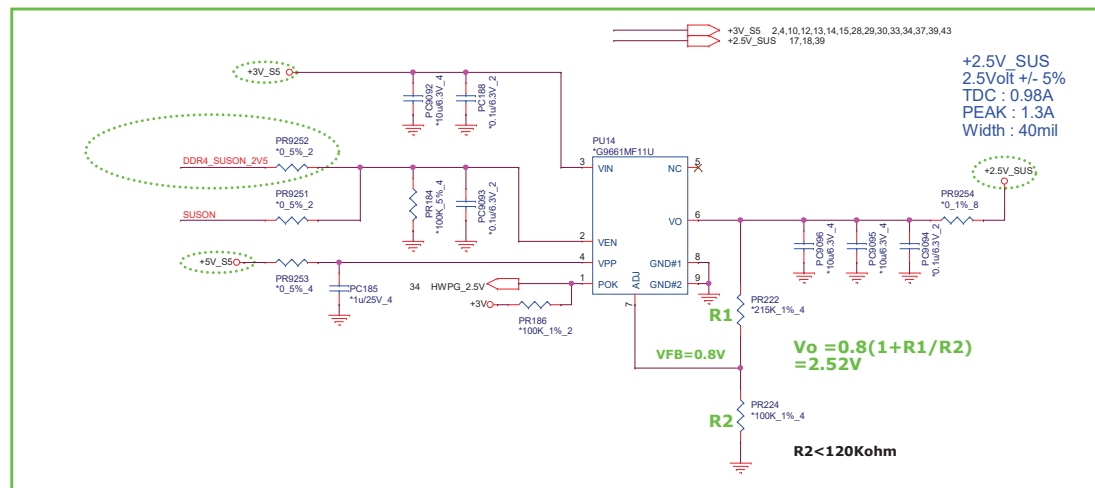
REGN MAX voltage 6.5V
 $V_{ILIM} = 20 * (V_{SRP} - V_{SRN}) = 20 * I_{chg} * R_{sr}$
 $= 0.793V$ for 3.965A current limit
 $I_{LIM} = 0.793V$
 $R_{sr} = 0.01ohm$







+2.5VSUS Power Rail For DDR4

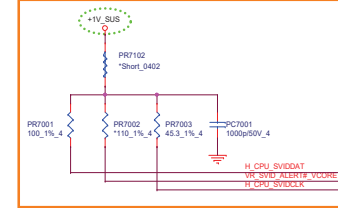


+VCC_CORE	5.741
+VCCGT	7.42
+VCCSA	6.42
+V_SUS	6.38
+VCCD	2.636,38.43
+V_S5	24.29,35.37,39.41,42.44,45.46
+V	2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,43,44,45,46

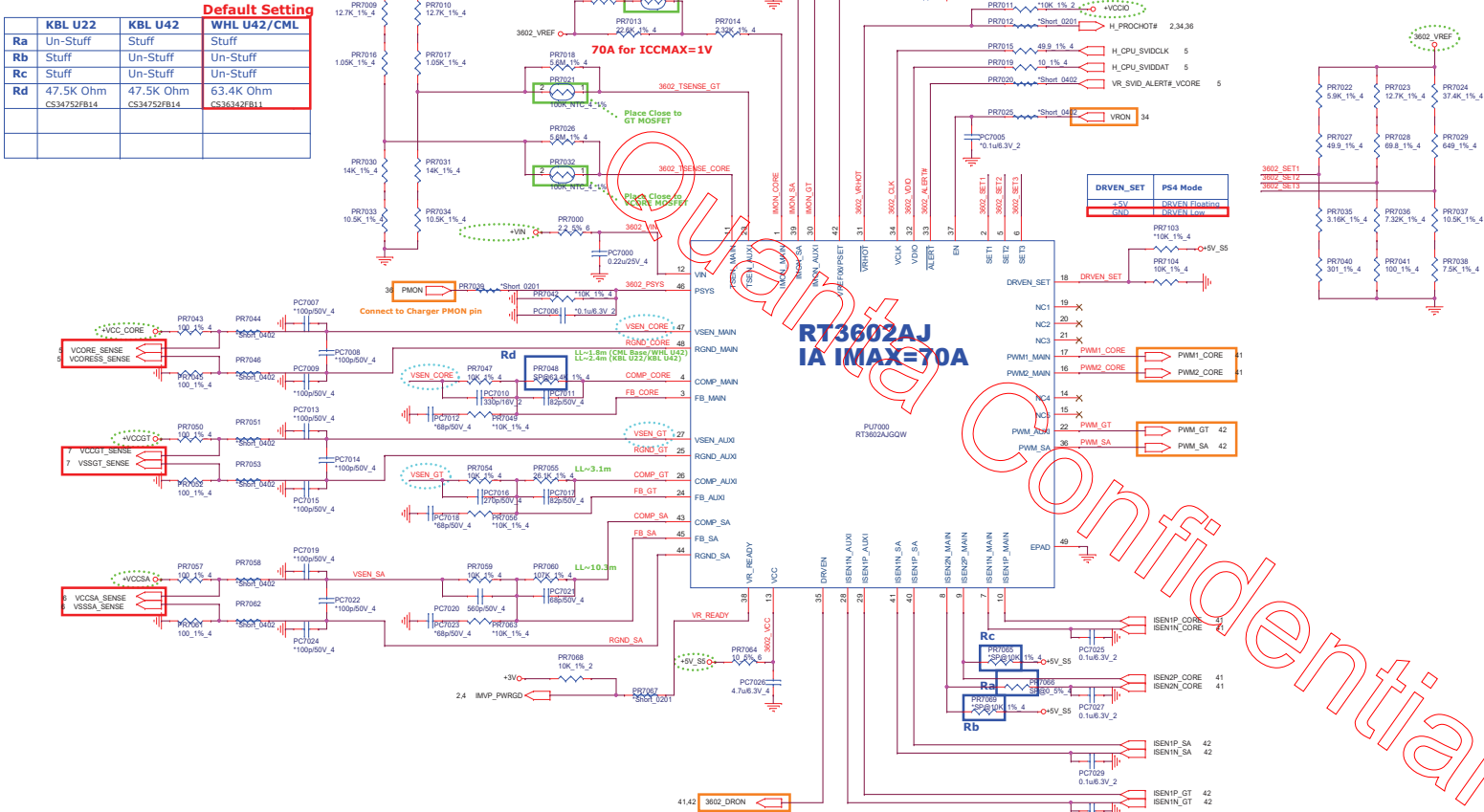
31A for ICCMAX=1V

6A for ICCMAX=1V




70A for ICCMAX=1V

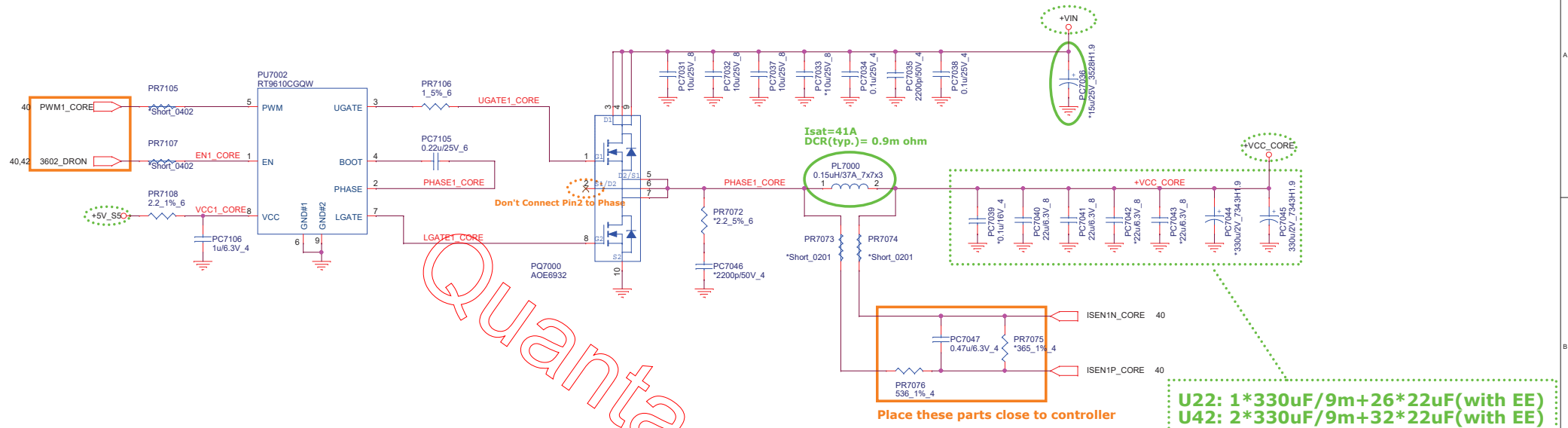
RT3602AJ
IA IMA=70ADouble Check SVID Setting With HW
(Pull high/Series R)

	KBL U22	KBL U42	WHL U42/CML
Ra	Un-Stuff	Stuff	Stuff
Rb	Stuff	Un-Stuff	Un-Stuff
Rc	Stuff	Un-Stuff	Un-Stuff
Rd	47.5K Ohm CS34752FB14	47.5K Ohm CS34752FB14	63.4K Ohm CS36342FB11

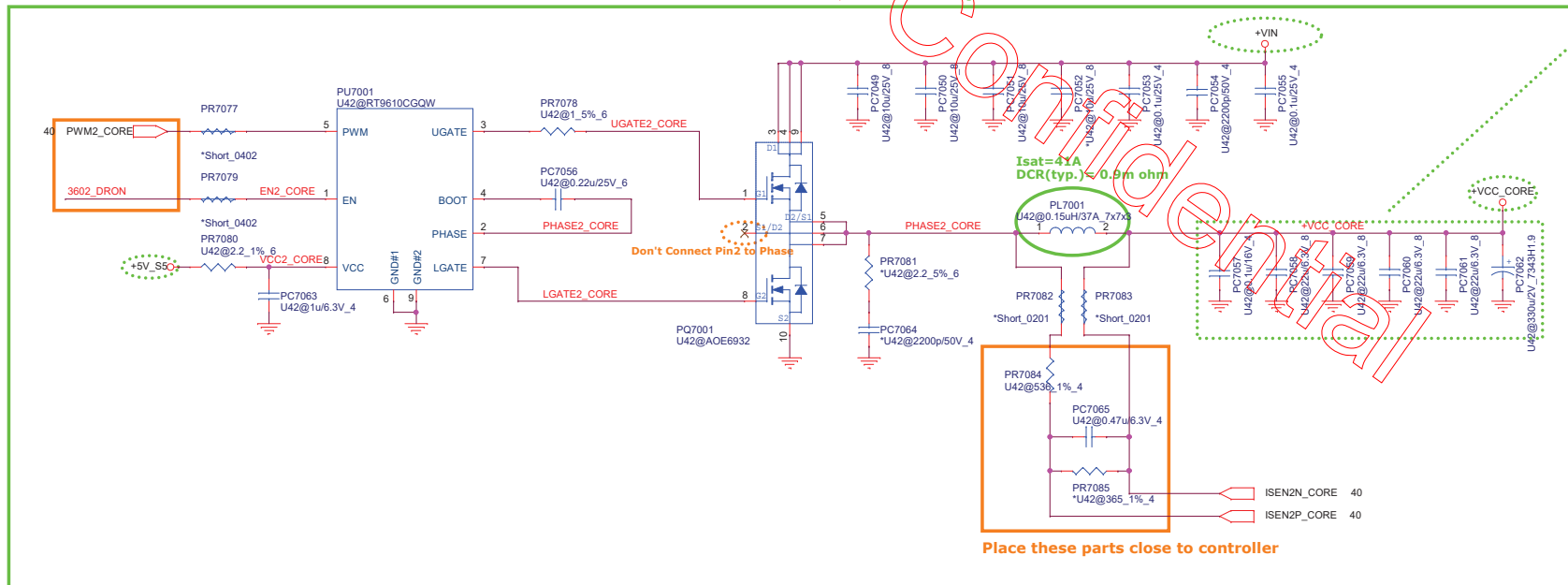


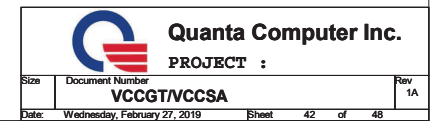
KBL - R (U22/U42)		WHL U42/CML Base
U22 (1+1+1 Phase)	U42 (2+1+1 Phase)	(2+1+1 Phase)
Vcore Icc Max : 32A Icc TDC : 21A OCP : 50A	Vcore Icc Max : 64A Icc TDC : 42A OCP : 100A	Vcore Icc Max : 70A Icc TDC : 48A OCP : 100A
VCCGT Icc Max : 31A Icc TDC : 18A OCP : 50A	VCCGT Icc Max : 31A Icc TDC : 12A OCP : 50A	VCCGT Icc Max : 31A Icc TDC : 18A OCP : 50A
VCCSA Icc Max : 6A OCP : 10A	VCCSA Icc Max : 6A OCP : 10A	VCCSA Icc Max : 6A OCP : 10A


 +VIN 25,36,37,38,39,40,42,43,44,45,46

 +VCC_CORE 5,7,40

 +5V_S5 24,29,35,37,39,40,42,44,45,46

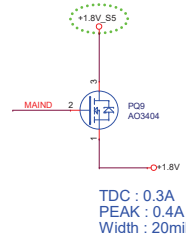
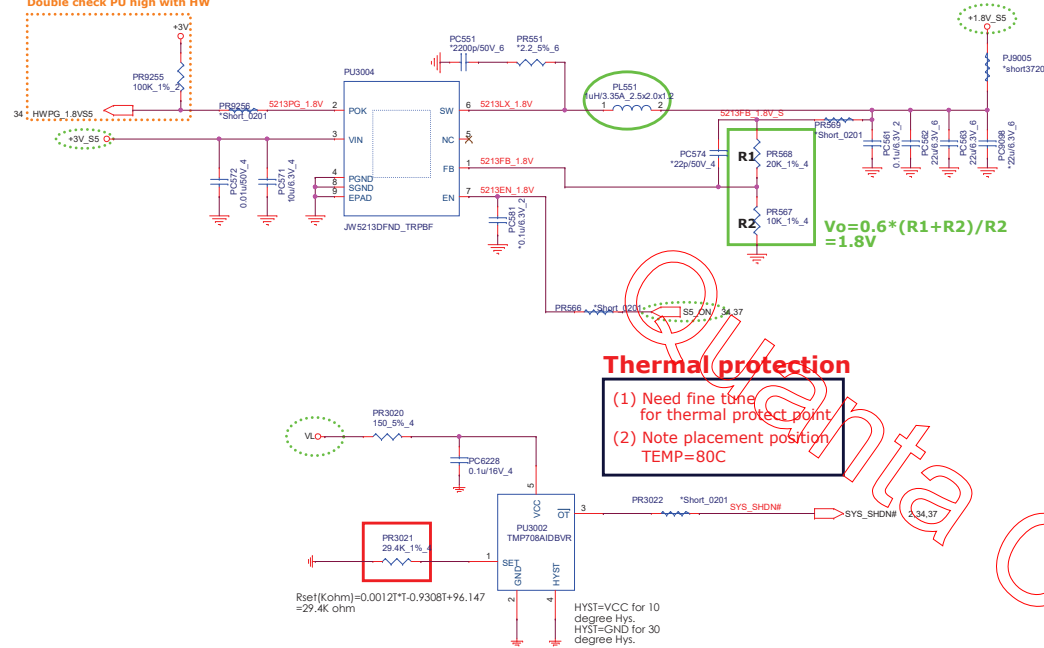


Vcore = 2 Phase for KBL-R U42/WHL U42/CML Base, 上件

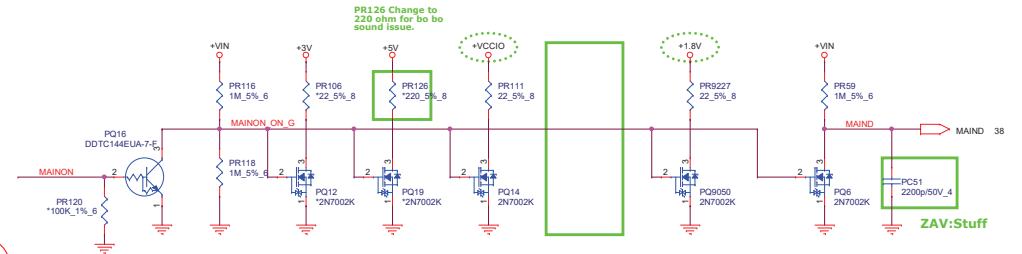
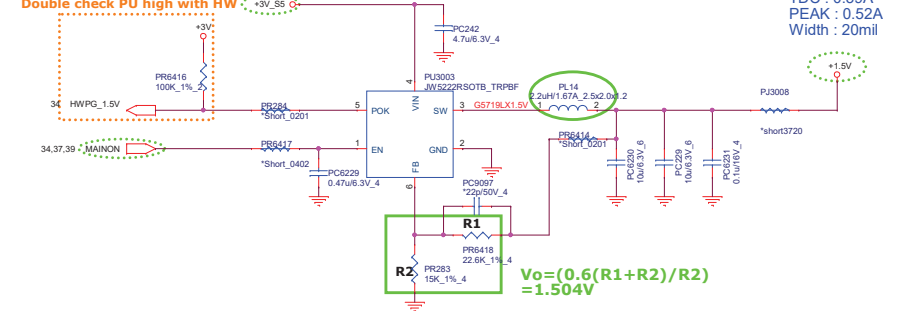




Double check PU high with HW

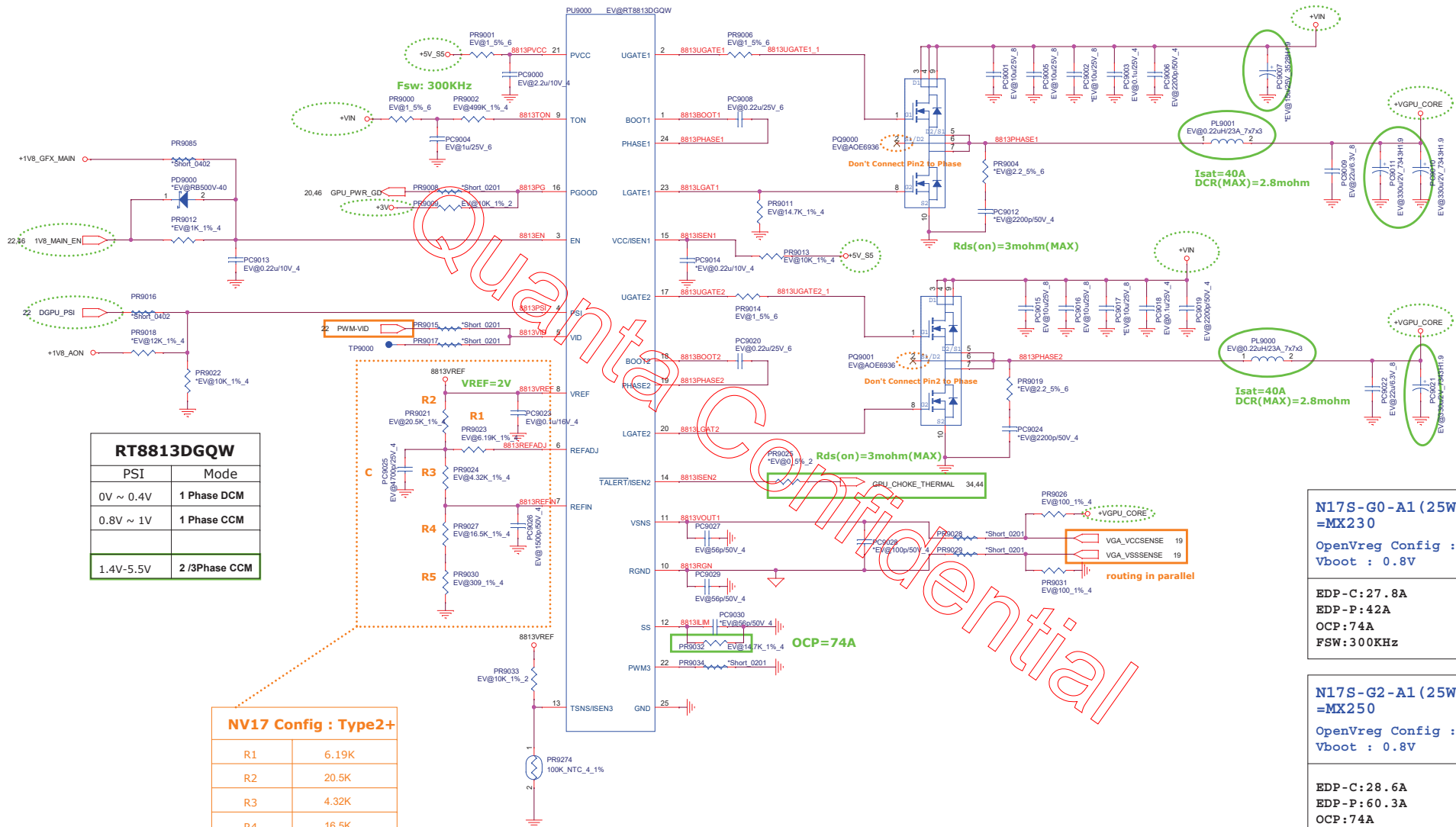


Double check PU high with HW



Vinafix

+VIN 25,36,37,38,39,40,41,42,43,45,46
 +VGPU_CORE 19
 +5V_S5 24,29,35,37,39,40,41,42,45,46
 +1V8_AON 19,21,22,46
 +1V8_GFX_MAIN 19,20,21,46
 GPU_CHOKE_THERMAL 34,44



N17S-G0-A1 (25W/GDDR5)
 =MX230

OpenVreg Config : Type2+
 Vboot : 0.8V

EDP-C:27.8A
 EDP-P:42A
 OCP:74A
 FSW:300KHz

N17S-G2-A1 (25W/GDDR5)
 =MX250

OpenVreg Config : Type2+
 Vboot : 0.8V

EDP-C:28.6A
 EDP-P:60.3A
 OCP:74A
 FSW:300KHz



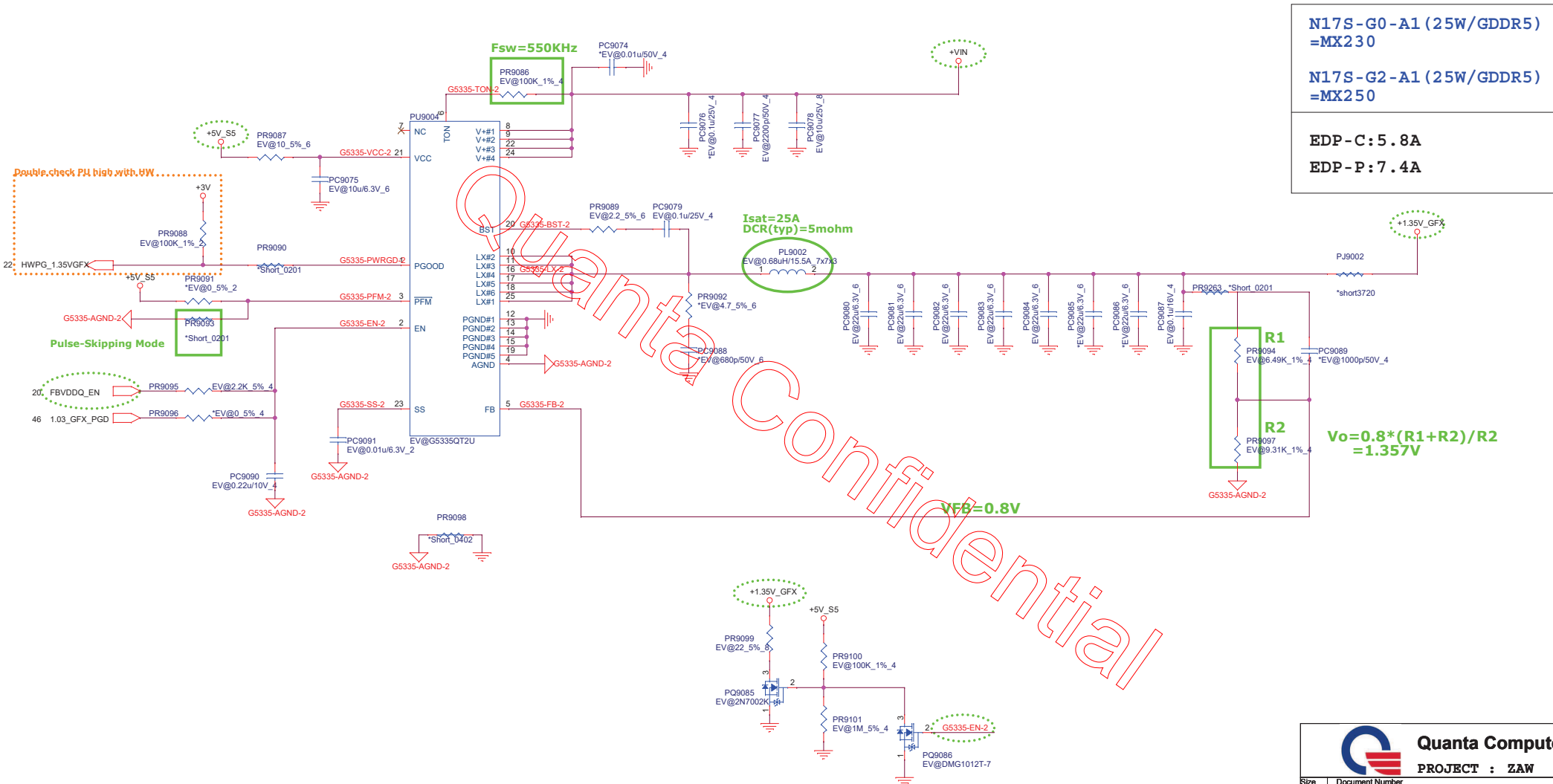
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Size Document Number
 +NVVDD (RT8813DGQW)
 Date: Wednesday, February 27, 2019 Sheet 44 of 48

1.35V_GFX

33

+VIN 25,36,37,38,39,40,41,42,43,44,46
+1.35V_GFX 20,23
+5V_S5 24,29,35,37,39,40,41,42,44,46
+3V 2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,43,44,46

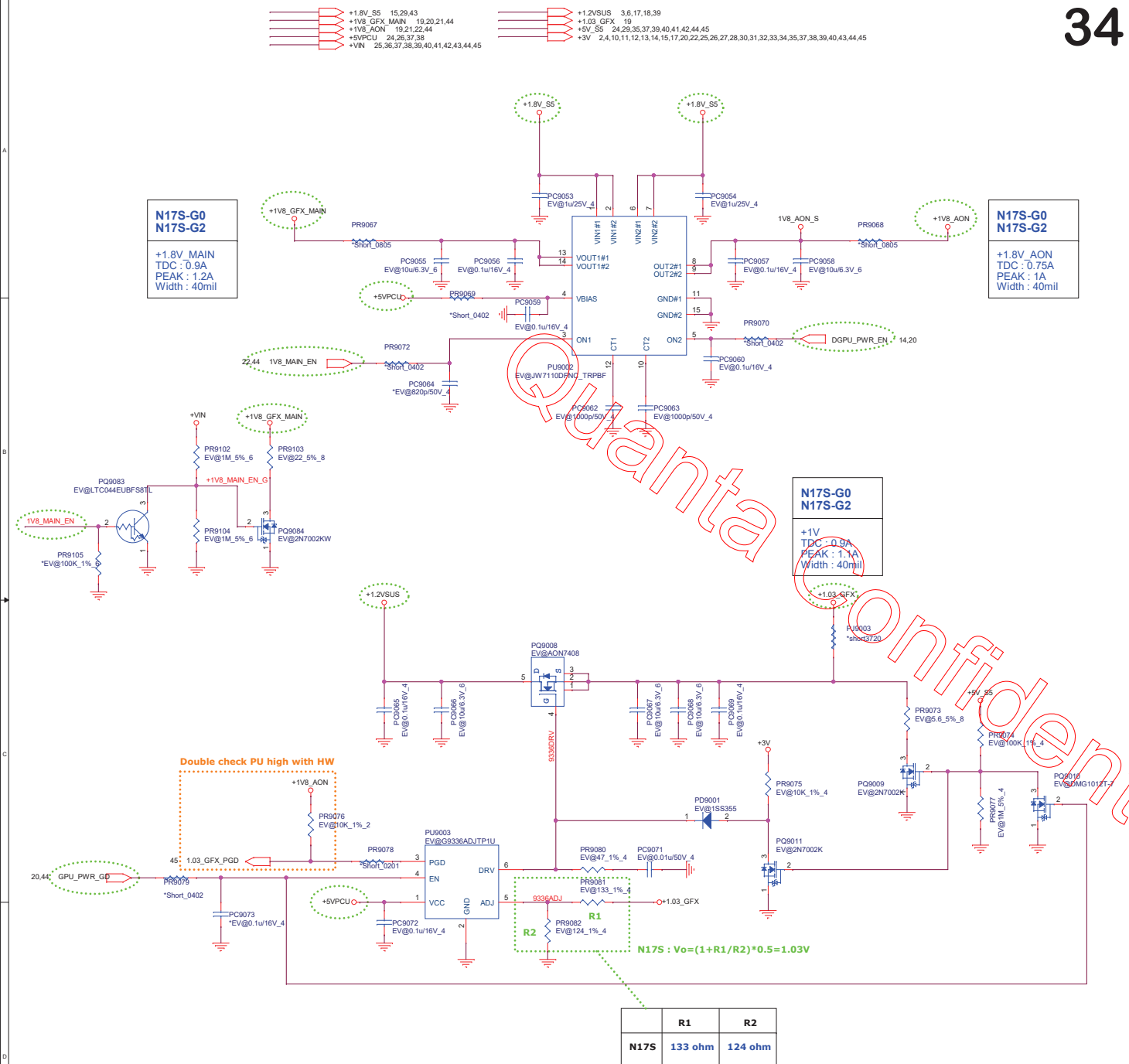


N17S-G0-A1 (25W/GDDR5)
=MX230

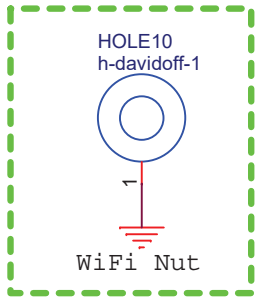
N17S-G2-A1 (25W/GDDR5)
=MX250

EDP-C: 5.8A

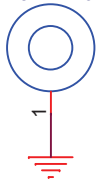
EDP-P: 7.4A



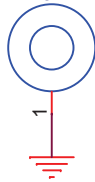
Hole



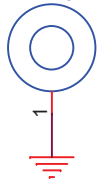
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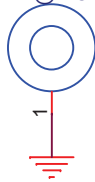
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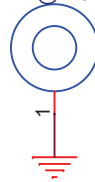
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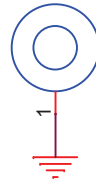
HOLE5
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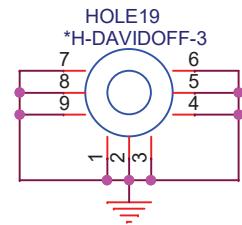
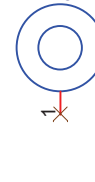
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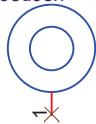
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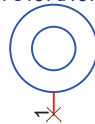
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HOLE12
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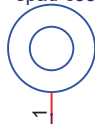
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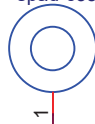
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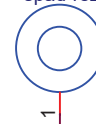
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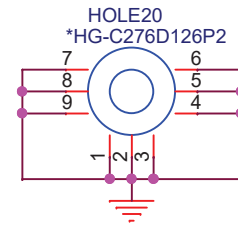
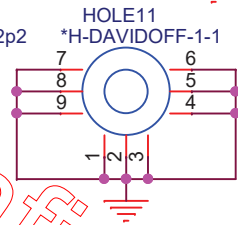
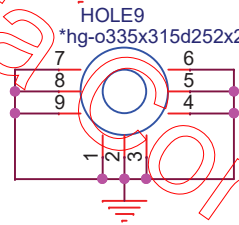
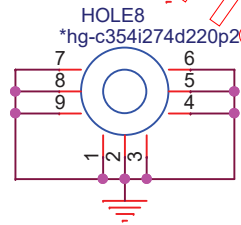
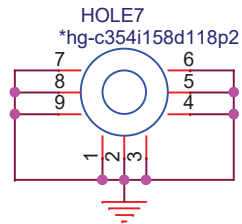
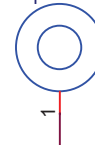
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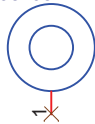
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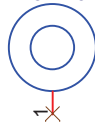
HOLE18
*spad-davidoff-1



HOLE23
*h-c98d98n



HOLE24
*h-s157d157n



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